Enabling Energy-Efficient Nonvolatile Computing With Negative Capacitance FET

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***Abstract*— Negative capacitance FETs (NCFETs) have attracted significant interest due to their steep-switching capability at a low voltage and the associated benefits for implementing energy-efficient Boolean logic. While most existing works aim to avoid the I_D–V_G hysteresis in NCFETs, this paper exploits this hysteresis feature for logic-memory synergy and presents a custom-designed nonvolatile NCFET D flip-flop (DFF) that maintains its state during power outages. This paper also presents an NCFET fabricated for this purpose, showing <10 mV/decade steep hysteresis edges and high, up to seven orders in magnitude, R_{DS} ratio between the two polarization states. With a device-circuit codesign that takes advantage of the embedded nonvolatility and the high R_{DS} ratio, the proposed DFF consumes negligible static current in backup and restore operations, and remains robust even with significant global and local ferroelectric material variations across a wide 0.3–0.8 V supply voltage range. Therefore, the proposed DFF achieves energy-efficient and low-latency backup and restore operations. Furthermore, it has an ultralow energy-delay overhead, below 2.1% in normal operations, and operates using the same voltage supply as the Boolean logic elements with which it connects. This promises energy-efficient nonvolatile computing in energy-harvesting and power-gating applications.**

***Index Terms*— Ferroelectric FET, hysteresis, negative capacitance FET (NCFET), negative capacitance, nonvolatility, nonvolatile computing, nonvolatile D flip-flop (DFF).**

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I. Introduction

NONVOLATILE computing has been an effective emerging solution to prevent computation progress loss due to either an unexpected or scheduled power outage. This is achieved by backing up memory and D flip-flop (DFF) states to on-chip nonvolatile memory (NVM) elements [1]–[6]. This technique is particularly useful for energy harvesting Internet-of-things (IoT) applications where frequent check-pointing is required under the notoriously intermittent supply provided by energy harvesting mechanisms [2]–[4]. Similarly, *in situ* backup also provides more energy savings in power-gating applications [1].

Several embedded NVM options, such as pulse-code modulation, spin-transfer torque magnetic random access memory, Resistive random access memory, and Resistive random access memory (ReRAM) have been proposed, as nonvolatile replacements for existing volatile embedded memories [7]. However, even with significant recent improvements [8]–[14], existing nonvolatile DFFs (NV-DFFs) need a significant amount of energy and time for one backup and restore operation. One factor in these high overheads is the duplicated backup and restore interface circuitry for each NV-DFF so as to convert the capacitance or resistance into a Boolean voltage [8], [11]. Another factor is the limited resistance ratio between different states and device variations in existing NVM devices which result in over-design to obtain a satisfactory yield. For example, when a global write control is applied, the write time of ReRAM devices should be not less than that of the slowest ReRAM device, resulting in unnecessary power consumption by faster devices [34]. The need for a high voltage or current to access the nonvolatile devices also brings additional overheads in power supply management, and may cause a peak power problem that limits the plausible number of parallel backup and restore operations [31]–[33].

The recent advent of negative capacitance FETs (NCFETs), also known as ferroelectric FETs heralds a new era of logic-NVM synergy. Being fundamentally different from existing NVM devices, NCFET can behave concurrently as an NVM and a logic device with inherent compatibility with Boolean signaling, which greatly reduces the complexity and energy consumption of the interface with logic gates. More importantly, unlike magnetic tunnel junction (MTJ) and ReRAM, there can be no static current during a write operation for NCFET memory. NCFET devices are being actively developed

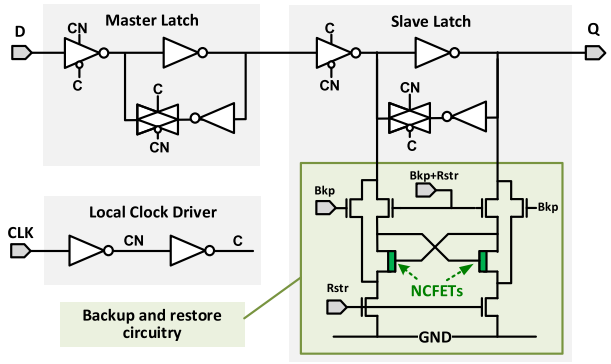

Fig. 1. Proposed NCFET NV-DFF for nonvolatile computing.

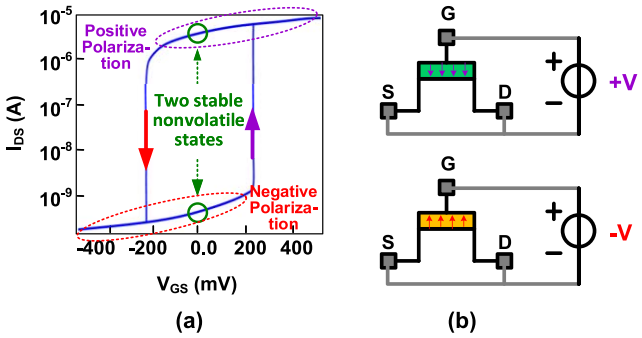

Fig. 2. Required NCFET characteristics. (a) I_D–V_G hysteresis with two stable nonvolatile states at $V_{GS} = 0$. (b) Polarization switching by the gate voltage. The I–V curve is obtained based on the LK-equation modeling method in [23], with 10-nm PTM CMOS FinFET as the integrated MOSFET. The LK-equation coefficients are: $\alpha = -1.05e9$ m/F, $\beta = 1e7$ m^5/F/coul^2, $\gamma = 6e11$ m^9/F/coul^4.

and explored for low-power Boolean logic [16]–[22], [27], [28]. Our recent NCFETs exhibit a steep hysteresis edge and a high ratio between the two I_{DS} states at $V_G = 0$, and confirm the potential of synergizing NVM and efficient logic with NCFET.

In this paper, we propose an NCFET NV-DFF in Fig. 1, with ultralow energy and latency in backup and restore operations and negligible energy-delay overhead in normal operations. Device-circuit codesign efforts have been made to harness the unique NCFET device features for performance optimizations.

II. Preferred NCFETs and Experiments

For the purpose of backup, restore, and nonvolatile states storage, the NCFETs in the NV-DFF are designed to have two locally stable states in the hysteresis around $V_G = 0$, as shown in the N-type I–V curve example in Fig. 2(a). One state can switch to the other by applying a sufficiently high-amplitude positive or negative V_{GS} that exceeds the coercive voltage [22], as shown with an N-type NCFET in Fig. 2(b). The state transition speed will be discussed in Sections III and IV.

Capacitance matching is critical to obtain the device characteristics in Fig. 2. In recent reports, NCFETs exhibit hysteresis when $|C_{FE}| < C_{MOS}$, where C_{FE} is the negative ferroelectric capacitance and C_{MOS} is the MOSFET gate capacitance [17], [18], [20]. In [19], hysteresis is found around $V_G = 0$ with about $100 \times I_{DS}$ ratio between the two hysteresis states. While these works try to avoid

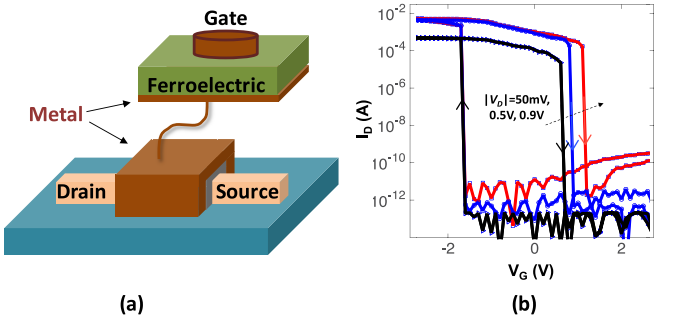

Fig. 3. P-type NCFET with externally connected $BiFeO_3$ ferroelectric material. (a) Device structure. (b) Measured I_D–V_G hysteresis around $V_G = 0$.

the hysteresis for Boolean logic operations, in this paper, we present an NCFET device with wide hysteresis around $V_G = 0$, as shown in Fig. 3(a). $BiFeO_3$ ferroelectric material was externally connected to a fin-structure field-effect transistor (FinFET) of 100-nm gate length. Fabrication and measurement follow the process in [17] but differ in the additional V_{TH} shifting in the baseline MOSFET to locate the hysteresis window around $V_G = 0$. Further work on more V_{TH} shifting could achieve the optimum goal of centering the hysteresis at $V_G = 0$.

Nevertheless, the key contribution of the device is the first experimentally verified NCFET, showing that: 1) shifting of the NCFET hysteresis curve by V_{TH} engineering to provide extra nonvolatility, as compared with its predecessor in [17] and 2) steep hysteresis edges with a slope below 10 mV/decade for above seven orders in magnitude between the two I_{DS} hysteresis states at $V_G = 0$. As to be revealed in this paper, a steep-slope transition edge provides a wide gate voltage range in which the polarization stays stable against noise; A higher ON-state current and a lower OFF-state current provides faster restore and immunity to device variations. These characteristics are preferred and well-captured in the proposed NV-DFF design.

III. Proposed NV-DFF Theories and Optimizations

A. Normal and Backup/Restore Operations

The proposed NV-DFF in Fig. 1 has a main body (the same as a conventional DFF consisting of a master latch and a slave latch), and an accessory circuitry connecting to the slave latch for backup and restore purposes. All backup and restore operations are associated with the slave latch only. In Fig. 1, *Bkp* is the backup operation control signal, and *Rstr* is the restore operation control signal. When both *Bkp* and *Rstr* are low, the interface transistors between the main body and the auxiliary circuitry are turned OFF by the gate signal *Bkp* and*Rstr*, leaving the main body functioning the same as a conventional positive-edge triggered DFF.

Fig. 4(a) shows the circuit state transition in the slave latch during a backup operation. When a supply outage is about to come, the backup control signal *Bkp* becomes high and turns ON the interface transistors $M1$–$M4$. Note that the pull-down transistors $M7$ and $M8$ gated by the restore control signal *Rstr* are turned OFF. Assuming Q is "1" (corresponding to a high voltage, V_{DD}) and QN is "0" (corresponding to GND), the feedback network quickly biases the two NCFETs

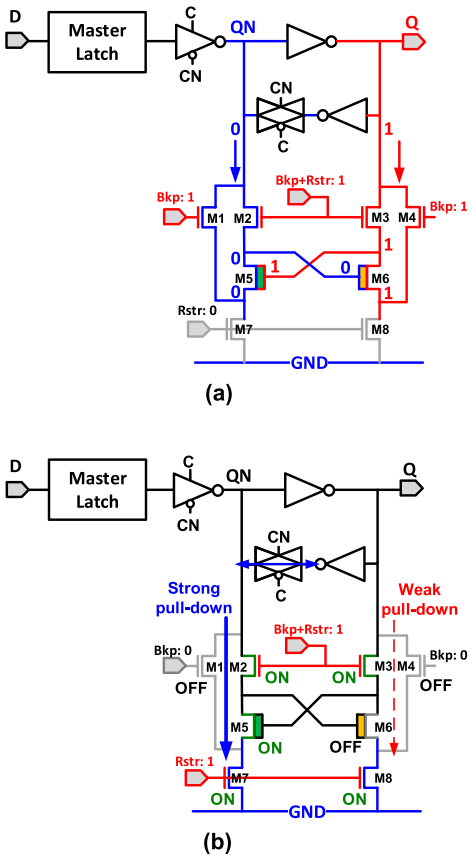

Fig. 4. (a) Circuit theory for backup operation and (b) restore operation.

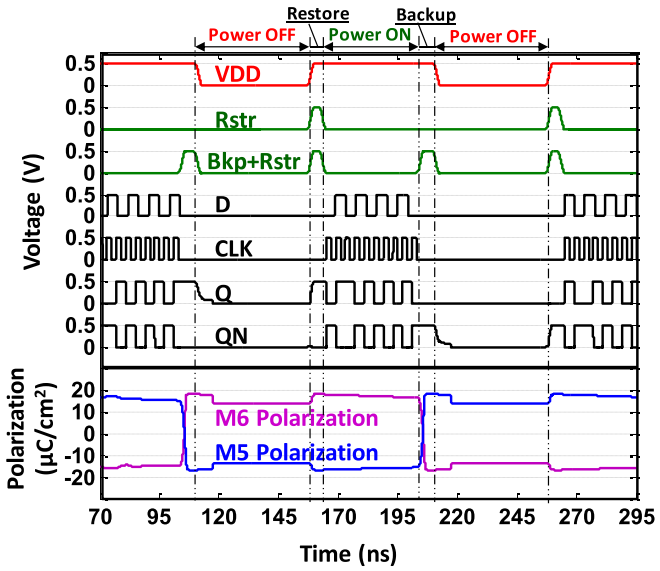

Fig. 5. Transient waveform snapshots of proposed NV-DFF with the CLK period equal to ∼4 ns during normal "power ON" operations. A few nanosecond after power supply goes OFF, the internal nodes like Q and QN are manually pulled down to ground to mimic real scenarios (this leads to faster settling down of the polarization as shown).

to switch to (or maintain) a positive polarization for $M5$ and a negative polarization for $M6$, respectively. The polarization switching is straightforward as their gates are biased at voltage levels opposite to their drain and source terminals: V_{DD}–V_{TH} for a high voltage level and GND at a low level. After the polarization switching is accomplished, removing V_{DD} will not affect the stored polarization states, regardless of *Bkp* and *Rstr* control signal levels. Note that the backup operation does not need to change the polarization if the state of the previous backup is the same. Operations with Q equal to "0" are similar.

Fig. 4(b) shows the circuit state transition for a restore operation. During the entire restore operation, the input clock signal CLK and backup control signal *Bkp* are set to be low (C = "0" and CN = "1"), and *Rstr* is set to be high. This guarantees that the slave latch is isolated from the master latch. As a result, the sensed resistance from Q and QN to GND and V_{DD} determines the final settled Q and QN voltage levels. For the positively polarized NCFET, its drain-to-source resistance is the order of magnitude lower than the other negatively polarized NCFET, which leads to a much stronger pull-down effect on the settling of its branch. The positive feedback network further enhances the difference, and finally leads to a full settling down as V_{DD} recovers.

Fig. 5 is a transient waveform snapshot, showing operations with a steady V_{DD} and backup and restore operations due to power failures. In the snapshot, the clock frequency is 0.25 GHz when the power supply is stable. It could be much faster as the isolated accessory backup and restore circuitry has negligible impact on the normal operation. To prevent the backup and restore operations from being interrupted, CLK is being kept low. The polarization state, as shown in Fig. 5, keeps stable in the power-off periods. Thanks to the simple timing requirement and the small control load, there is no need for a second supply network to deliver power for the control signals.

Note that the proposed NV-DFF backup and restore circuitry could also be built with P-type transistors connecting to V_{DD} with effective control signals at a low voltage.

B. Device-Circuit Co Design

From the device's perspective, given the ferroelectric material, the NCFET parameters can be tuned by the ferroelectric layer thickness T_{FE} and the ferroelectric layer area A_{FE}. From the perspective of circuits and applications, the desired performance features mainly include energy-delay overhead during normal operations, backup and restore energy and delay, retention time, yield and reliability, etc.

The backup and restore energy is one key specifications of NV-DFF. For energy-harvesting systems with an intermittent power supply, it limits the overall energy efficiency as more energy spent for backup and restore operations results in less energy for computation. For check-pointing applications, the backup and restore energy indicates a certain period of power-off time, i.e., break-even time (BET), below which no energy savings could be achieved. The backup and restore time is also critical for some applications when a fast response is preferred, e.g., fine-time-granularity power-gating scenarios and fast response processors.

Fig. 6 shows how T_{FE} and A_{FE} affect the NCFET device I–V characteristics and the NV-DFF performance. Increasing T_{FE} increases the coercive voltage or energy barrier to flip the polarization, leading to longer retention time and more time to switch the polarization. A larger T_{FE} reduces the restore time with a higher ON/OFF resistance ratio and a lower

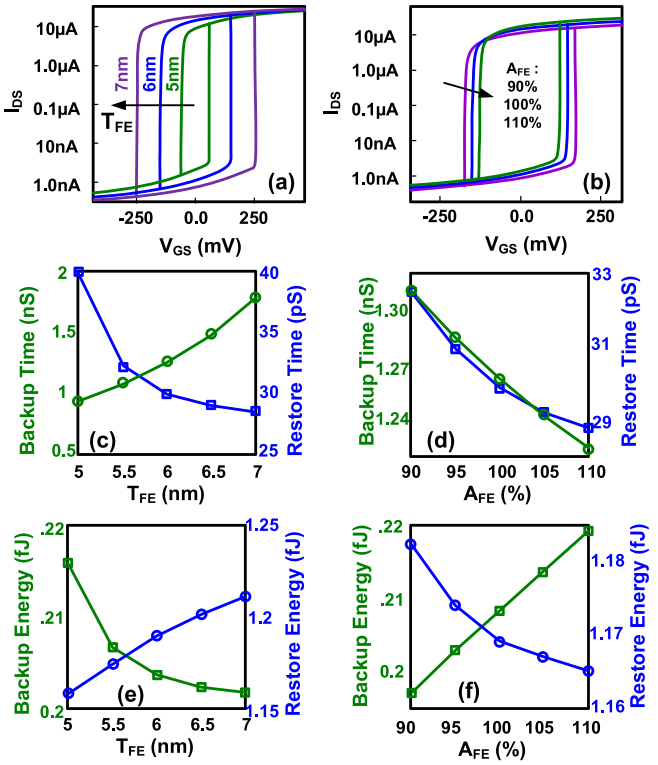

Fig. 6. Impact of varying T_{FE} (baseline 6 nm) and A_{FE} (baseline 100% of 378 nm^2) on NCFET I_{DS}–V_{GS} in (a) and (b), NV-DFF backup and restore time in (c) and (d), NV-DFF backup and restore energy in (e) and (f). V_{DD} is 0.5 V. The kinetic coefficient ρ is 0.25. The device parameters are the same as shown in Fig. 2. More simulation settings are in the next section.

ON-state resistance. The variation of T_{FE} from 5 to 7 nm also slightly affects the backup and restore energy by less than 10%. Meanwhile, decreasing A_{FE} also changes the capacitance matching between C_{FE} and C_{MOS}, leading to a different I–V with a higher coercive voltage, a lower ON-state current, and longer polarization switching time.

Considering the inevitable T_{FE} and A_{FE} variations in the fabrication process, T_{FE} and A_{FE} should be carefully optimized considering the supply voltage range, the retention model, and the application requirements on the retention time, backup and restore energy, and latency. While it varies from case-to-case, in this design evaluation, T_{FE} and A_{FE} are set to be 6 nm and 378 nm^2 (equal to 3$*$ fin_width$*$channel_length) for one fin, respectively, for the optimized trade off. These parameter values, unless otherwise stated, will be used in the performance evaluation in Section IV.

IV. NV-DFF Performance

This section describes SPICE simulations and performance comparisons. More variation and yield analysis, and future work are also covered.

A. Simulation Settings and Baseline Designs

The physics-based ferroelectric capacitance model in [23] is employed to build NCFETs with 10-nm PTM CMOS FinFET as the integrated MOSFET. In this model, the ferroelectric material has been calibrated by experimental results of lead zirconium titanate (PZT) films on hafnium oxide (HfO_2)

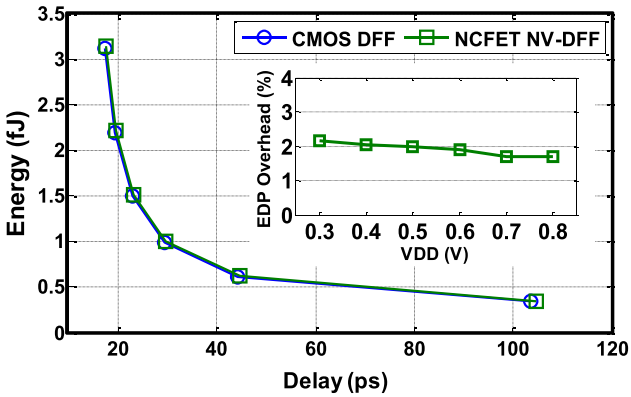

Fig. 7. Energy-delay performance overhead of the proposed NCFET NV-DFF under a supply voltage from 0.30 to 0.80 V. The kinetic coefficient ρ is 0.25.

buffer. To reflect different polarization switching speed, in the NCFET model, the kinetic coefficient ρ is varied from 0.04 to 0.25. A typical value of $\rho = 0.25$ has been adopted as in [15], [23], and [26]. The baseline CMOS volatile DFF is optimized with the minimum area and a similar clock-to-Q delay between "0" and "1" outputs (the number of fins for nMOS and pMOS is 1 and 2, respectively). The DFFs are simulated with a 2 fF load and 20 ps rising and falling time for D and CLK inputs.

B. Energy-Delay Overhead

For the NV-DFF in many applications, energy-delay performance remains critical because the DFF is still operating with a steady supply for a large portion of time. Therefore, it is meaningful that the additionally acquired nonvolatility does not cause high energy-delay overheads. Fig. 7 shows these overheads over the baseline CMOS volatile DFF design. Due to the normally-OFF configuration of the backup and restore circuitry, the energy-delay product (EDP) overhead is lower than 2.1% for V_{DD}s above 0.4 V. If a larger-size baseline DFF is used, this EDP overhead becomes even more negligible, because the backup and restore circuitry need not be scaled up by the same ratio due to the low (high) OFF-state (ON-state) NCFET resistance. In addition, thanks to the normally-OFF configuration, the backup and restore operations have little impact on the DFF setup time and hold time requirement.

C. Variation and Noise Performance

Existing NVM and NV-DFF designs suffer from the non-idealities of the nonvolatile storage devices inside, especially the variations and low resistance ratio between different states of resistive memory devices, such as MTJ and ReRAM [11], [30], [31], [34]. In such approaches, the worst-corner devices often greatly limit the overall system performance. For example, as mentioned in Section I, the ReRAM write pulse duration is much longer than average to ensure yield, resulting in high energy consumption. Therefore, it is important to analyze how the NV-DFF performs with NCFET variations.

Fig. 6 has actually shown how the NV-DFF behaves with global T_{FE} and A_{FE} variations (all devices vary from the design

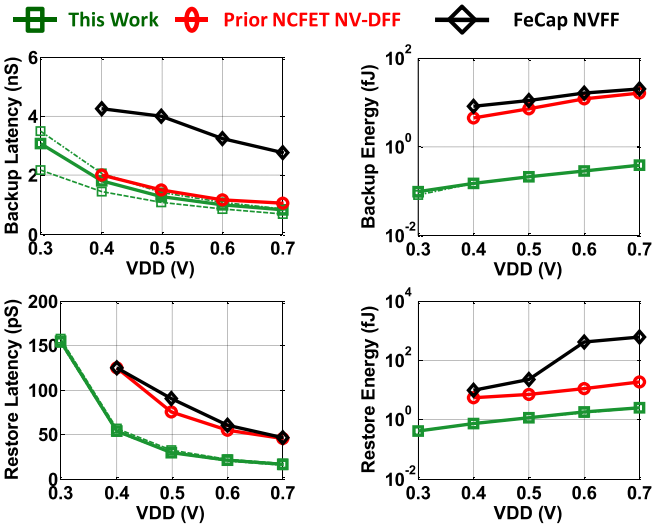

Fig. 8. Performance of backup and restore energy and latency evaluations, in comparison with previous NV-DFF in [15] based on ferroelectric capacitor (black) and a prior NCFET circuitry (red). Three sets of data in green are included, considering NCFET T_{FE} mismatches in one NV-DFF in three combinations: 6 nm/6 nm (no mismatch), 6 nm/5.5 nm, 6 nm/6.3 nm. The kinetic coefficient ρ is 0.25.

target by the same amount). Here more scenarios are provided, considering local mismatches, i.e., the two NCFETs in one NV-DFF having different T_{FE}. In Fig. 8, the green curves are for three sets of the proposed NCFET NV-DFF results operating in a range of V_{DD} with T_{FE} diverting away from 6 nm by -10% to $+5\%$. These simulation results show that the major impact is on the backup latency in low V_{DD} scenarios, while the impact on other metrics is comparatively much less significant than that brought by a different supply voltage.

The impact of additional noise that causes a nonzero initial Q/QN voltage opposite to the desired value is also analyzed through comprehensive simulations. We found that noise up to 200 mV is fully tolerable for correct operations, even with the above mentioned local NCFET mismatches. Such unwanted initial charge at Q or QN will be quickly discharged by the restore branches. Proper timing, the low ON-state and high OFF-state resistance of the NCFETs at different polarization states enable this feature.

As indicated by [23] and [29], the kinetic coefficient ρ affects the polarization switching time significantly. Different practical kinetic coefficient values are adopted in simulations to reflect different polarization switching time, as shown in Table I. This also indicates the value of material and device research in making faster NCFETs.

D. Performance Comparisons

Fig. 8 compares the backup and restore performance with existing NV-DFF designs in [15]. The proposed NCFET NV-DFF exhibits more than 6× reduction in the restore energy and 30× reduction in the backup energy. It also performs better in backup latency, and significantly outperforms the others with more than 50% reduction in restore latency. In addition, the proposed NV-DFF works with general DFFs based on master-slave latches, which is superior to the design in [15] that only works when the baseline DFF has set/reset ports. During restore operations, the design in [15] could not fully eliminate the static current of low-resistance-state NCFETs. The gains over the design in [15] stem from the deeply embedded logic-in-memory operation with the proposed simple circuit structure that can carry out the backup and restore operations in only one step without static current consumptions.

TABLE I
PERFORMANCE COMPARISONS AMONG RECENT NV-DFF DESIGNS

	[10] measured	[9] simulated	[11] simulated[&]	This Work simulated*		
Tech. size	130nm	70nm	180nm	10nm		
Voltage	1.5V	1.0V	1.8V	0.3V-0.8V		
Material	PZT Cap	MTJ	ReRAM	6nm HfO_2, PZT		
				ρ=0.04	ρ=0.10	ρ=0.25
$T_{Backup+Restore}$	2.67µS	>10uS	1.3µS	277ps	583ps	1.29ns
$E_{Backup+Restore}$	**2.40pJ**	**382fJ**	**735fJ**	**1.38fJ**		
Break-Even Time	/	**0.83µs@25°C**	**1.47ms**	**55.9ns**		

[&]: The results are for the topology of NVFF-I in [11] operating at 0.8 V supply (rise to 2.4V for ReRAM write) for the shortest break-even time.
*: Backup and restore performance in this table is simulated at 0.5V supply.

Table I also summarizes the NV-DFF overall performance in comparison with some other reported designs in different technologies. One of the strongest advantages of the proposed NV-DFF over others is the orders of magnitude lower energy for backup and restore operations. Such energy savings partly come from the capability of NCFETs to operate effectively at a lower voltage. Two more important factors are: 1) the fundamentally different three-terminal NCFET device operating in a novel cross-coupled circuitry that avoids static NCFET drain–source current during backup and restore operations and 2) NCFETs of a small size that can still ensure fast and robust operations with a high ON/OFF state resistance ratio even in the presence of significant local and global variations. In contrast, existing resistive memory elements in reported NV-DFF designs, such as MTJ and ReRAM, are continuously drawing current (because of their inherent two-terminal device feature) for a long period of time to ensure yield (because of required-write-time duration variations with a much lower resistance ratio). For capacitive NVM devices, such as ferroelectric capacitors in [10], their power inefficiency arises from a complex access interface and a large capacitance value.

The low-energy backup and restore operations in the proposed NV-DFF enable higher-efficiency nonvolatile computing applications. For energy harvesting systems with an intermittent supply, the saved backup and restore energy could be used for computing, leading to more forward progress, and higher quality of service. For general power-gating systems, the lower backup and restore energy leads to a shorter BET versus the leakage energy of an idle unit, indicating significant expansion of opportunity for energy savings from fine-grained power-gating.

E. Future Work

Beyond existing NCFET models in [23] and [24], future models that characterize the device variation, temperature

dependence, retention time, endurance and aging, etc., are required for more comprehensive evaluations. For example, retention time can be a key specification in some applications. In NCFETs, this is mainly determined by the coercive voltage, the remnant polarization, and the area of the ferroelectric layer. Aging may and may not be a limiter, depending on how frequent the backup operation occurs (usually orders lower in magnitude than the clock frequency).

Meanwhile, more NCFET device fabrication efforts that focus on better shaping the hysteresis could provide solid support for feature verification, model calibration, and circuit design. Future circuit optimizations and experiments for nonvolatile computing are also warranted.

Furthermore, while the proposed NCFET NV-DFF provides strong synergies for nonvolatile computing, it will be important to optimize the existing computing architectures accordingly [35], [36]. This is because the tradeoffs between retention time, operation energy, area, and yield will have shifted significantly from prior approaches.

V. Conclusion

This paper has proposed an approach to nonvolatile computing with NCFETs nonvolatile DFFs by harnessing the logic-NVM synergy with a novel circuitry. With negligible energy-delay overhead in the normal operation, low energy and low latency in backup and restore operations, it enables a new paradigm for future IoT and power-gating applications.

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