Tunnel FET RF Rectifier Design for Energy Harvesting Applications

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***Abstract*—Radio-frequency (RF)-powered energy harvesting systems have offered new perspectives in various scientific and clinical applications such as health monitoring, bio-signal acquisition, and battery-less data-transceivers. In such applications, an RF rectifier with high sensitivity, high power conversion efficiency (PCE) is critical to enable the utilization of the ambient RF signal power. In this paper, we explore the high PCE advantage of the steep-slope III-V heterojunction tunnel field-effect transistor (HTFET) RF rectifiers over the Si FinFET baseline design for RF-powered battery-less systems. We investigate the device characteristics of HTFETs to improve the sensitivity and PCE of the RF rectifiers. Different topologies including the two-transistor (2-T) and four-transistor (4-T) complementary-HTFET designs, and the n-type HTFET-only designs are evaluated with design parameter optimizations to achieve high PCE and high sensitivity. The performance evaluation of the optimized 4-T cross-coupled HTFET rectifier has shown an over 50% PCE with an RF input power ranging from −40 dBm to −25 dBm, which significantly extends the RF input power range compared to the baseline Si FinFET design. A maximum PCE of 84% and 85% has been achieved in the proposed 4-T N-HTFET-only rectifier at −33.7 dBm input power and the 4-T cross-coupled HTFET rectifier at −34.5 dBm input power, respectively. The capability of obtaining a high PCE at a low RF input power range reveals the superiority of the HTFET RF rectifiers for battery-less energy harvesting applications.**

***Index Terms*—Energy harvesting, power conversion efficiency, radio-frequency (RF)-powered systems, RF rectifier, steep subthreshold slope, tunnel field-effect transistors (FETs), III-V semiconductor.**

I. Introduction

RAPID progress in the development of energy harvesting systems with advanced sensing technologies and wideband transceivers have enabled a broad range of applications, such as implantable medical devices [1], [2] and wearable bio-activity monitoring platforms [3]–[5], etc. In these applications, the battery replacement with highly efficient radio-frequency (RF) power harvesters offers many advantages, which reduces the weight and cost of the system, and also eliminates the charging inconvenience and the risk of replacing the batteries [1]–[6]. Many works have investigated the CMOS passive radio-frequency identification (RFID) tags for harvesting the ambient RF signals [1], [3]–[6], where the ambient RF signal is converted to dc power through an RF rectifier. However, due to the limited ambient RF power in the environment and the challenges to achieve high power conversion efficiency (PCE) with the weak RF input power, existing RF-powered systems have limited data processing capabilities and operating ranges [3]–[6]. Fig. 1 presents the PCE versus RF input power in recently reported CMOS RF rectifier designs, where the PCE for below −30 dBm RF input (typical ambient RF-power range) is less than 20% [21]–[40]. Therefore, the design of a high-sensitivity, high-PCE RF rectifier is critical to achieve longer operation range and more functionality for RF-powered applications.

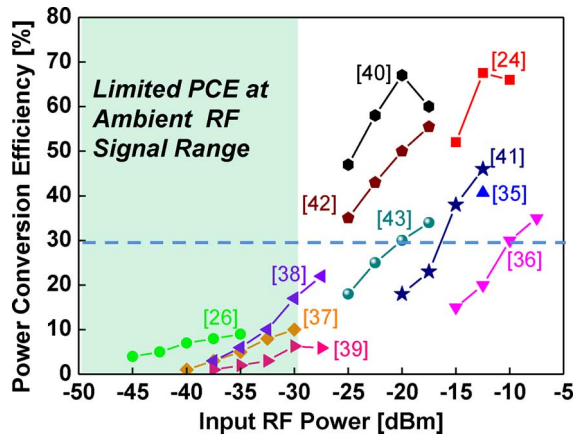

Fig. 1. PCE versus the input RF power from the recently reported CMOS RF rectifier designs for RFID and energy harvesting applications [24]–[43].

Steep-slope tunnel field-effect-transistors (tunnel FETs, TFETs) stand as one of the most promising candidates to mitigate the energy efficiency challenges of the conventional CMOS technology and further enable the supply voltage scaling below 0.3 V [7], [8]. By taking advantages of the band-to-band tunneling induced carrier injection mechanism, TFETs, in principle, are able to achieve a sub-thermal energy switching (sub-60 mV/decade) with a high on-off current ratio

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at reduced supply voltages. The advancement in the TFET on-current improvement with improved gate-electrostatic control, low-bandgap material and tunneling junction engineering [9]–[12], as well as the process development of the heterogeneous integrations [13] has shown its prominent potential to extend the technology roadmap with optimal energy efficiency beyond the CMOS limit. Lots of efforts have also been made on TFET-based circuit and architecture designs, compact model development, reliability evaluation, and variation analysis [14]–[18] to bridge the device innovations with the practical circuit and system design requirements. Moreover, TFET ultra-low power analog/RF circuit designs have recently attracted lots of interest, benefited from the steep-slope-induced transconductance to drain current ratio (g_m/I_{DS}) improvement, turn-on voltage reduction, uni-directional operation, as well as its desired low-voltage and high-frequency characteristics [19]–[21]. These unique device characteristics of TFETs could be utilized to improve the sensitivity range and the PCE in the RF-powered energy harvester designs.

In this work, we explore the GaSb-InAs heterojunction tunnel FET (HTFET) RF rectifier designs for energy harvesting applications. Based on the theoretical analysis of the HTFET device characteristics, we evaluate the performance advantages of the HTFET RF rectifiers to improve RF-power utilization ranges with high power conversion efficiency. We evaluate different topologies for HTFET rectifier designs with performance optimizations from the transistor sizing, coupling capacitances, and multi-stage configurations and compare with the baseline Si FinFET rectifier.

In the rest of this paper, Section II discusses the ongoing efforts of RF-powered energy-harvesting systems and the design challenges of CMOS RF rectifiers. Section III describes the TFET device designs and the HTFET advantages in improving RF rectifier sensitivity and PCE. Section IV presents different HTFET rectifier topologies with detailed operation mechanisms. The performance evaluations and optimizations of both single-stage and multi-stage rectifiers are discussed in Section V, followed by the conclusions in Section VI.

II. RF Rectifiers for Energy Harvesting Systems

A. RF Energy Harvesting for Battery-Less Applications

Low-power sensor technology advancements and circuit design techniques have enabled many applications powered by the RF signals in the ultra-high frequency (UHF) band. The power consumption of these systems ranges from a few microwatts to milliwatts. The work in [5] reports a 16~33 μW RF-powered temperature sensor with 37% PCE and -12 dBm signal sensitivity at 900 MHz. The 50.6 μW RF-powered biomedical transmitter with a data rate of 4 Mb/s in [6] shows -6 dBm sensitivity at 918 MHz and 20%~30% PCE. In [4], a 1.23 mW 5 Mb/s neural/EMG telemetry system achieves 20.6% PCE and an RF range of 1.5 m at a 4 W equivalent isotropically radiated power (EIRP). The recently developed glucose sensor in [3] consumes 3 μW power with 20% PCE and an RF range of 15 cm with a 10 W EIRP. Among all these designs, the operation range is stringently constrained by the overall system power consumption and limited PCE.

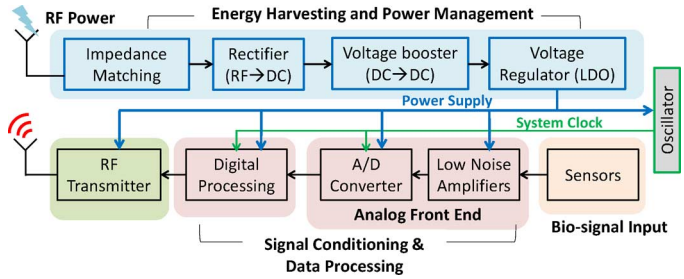

Fig. 2. Typical RF-powered system block diagram.

Fig. 2 illustrates the block diagram example of an RF-powered system, including the energy harvesting and power management block, the signal conditioning and data processing block, sensors, and an optional RF transmitter depending on the application [47]. The signal conditioning and data processing block includes the low-power analog/RF frontend, digital processing units, and oscillators for clock generation. The energy harvesting and power management block includes impedance matching networks, RF rectifier, optional dc-dc converter for voltage boosting, voltage regulator, and the energy storage unit. Because the entire system is powered by the dc output of the rectifier circuits, the design of a high-sensitivity, high-PCE RF rectifier is critical in these applications in order to increase the available dc power for the entire system operation.

B. Challenges of CMOS RF Rectifier Design

Many works have studied the CMOS RF rectifier design for RFID applications [19]–[24]. The diode-connected MOSFET Dickenson charge pump has been well explored as an alternative of the Schottky diode-based designs due to its desired process compatibility with the CMOS circuits. However, these designs suffer from the efficiency loss induced by a large threshold voltage V_{th} (or turn-on voltage $V_{turn-on}$) , hence the maximum PCE is relatively small [19], [20]. [22] has employed the voltage boosting technique in a sub-threshold CMOS Dickenson charge pump to optimize the dc output voltage with a sensitivity down to -32 dBm, whereas the PCE has not been studied. Derived from the Dickenson charge pump topology, a self-V_{th}-cancellation scheme is proposed in [20] for a 2-T CMOS rectifier (2-T SVC), which further improves the PCE up to 30% at -9.9 dBm RF input.

In both the diode-connected charge pump and SVC rectifier designs, the trade-off between the device turn-on voltage and the leakage power loss has significantly limited the PCE and sensitivity. The rectifier operation requires the RF signal voltage amplitude above the turn-on voltage of a transistor or a diode. When a transistor operates in the sub-threshold regime, a large on-state channel resistance R_{on} due to the drive-current reduction induces an increased voltage-drop on the rectifier, which leads to a high resistive power loss and a reduced output dc voltage and PCE. Therefore, a device with a small turn-on voltage (e.g., a low-V_{th} CMOS) is preferred to achieve a high-sensitivity rectifier. However, when reducing V_{th}, the reverse leakage current that flows from the output to the input or ground increases, which degrades the power efficiency [24].

Later, the 4-T cross-coupled CMOS rectifier [22], [24] with a dynamic-V_{th}-cancellation scheme has shown a significant improvement of PCE compared to the previous designs (e.g., 67.5% PCE at -12 dBm in [24]), which has been widely adopted by the UHF RFID applications. The dynamically biased transistor gate voltage provides an effective threshold voltage reduction at the transistor on-state while reducing the off-state leakage simultaneously. However, due to the nature of the sinusoid RF input, the transistors in the 4-T cross-coupled rectifier could be reversely turned-on, causing a reverse conduction induced power loss. Several works have proposed design modifications by adding additional transistors or "switches" to eliminate the reverse conduction issues to further improve the PCE [26], [27] (71.5% peak PCE at -4 dBm in [27]), but at an expense of increasing the circuit complexity. In general, for battery-less RF-energy harvesting applications, designing a rectifier with a high-sensitivity and a high-PCE to allow long-range communication with more computation capability remains challenging.

III. TFET Technology and its Advantages

A. The TFET Technology for Analog/RF Applications

TFET has emerged as a prominent candidate to mitigate the supply voltage scaling challenge [7], [8]. It employs the band-to-band tunneling carrier injection mechanism in a reserved biased, gated p-i-n diode with a field-effect control of the tunneling current. In conventional MOSFETs, the 60 mV/decade SS originates from thermionic emission of carriers, in which only the high energy carriers with energy exceeding the source-channel energy barrier contribute to the overall current. These high energy carriers exhibit an energy slope of kT (k is the Boltzmann constant, T is the absolute temperature) in Fermi-Dirac distribution, resulting in a thermal energy limited SS of $kT/q \cdot \ln 10$.

Unlike MOSFETs, the gate-controlled tunneling window in TFETs is able to effectively filter the high energy carriers in the energy bands and hence leads to a sub-60 mV/decade steep slope at the room temperature. In order to achieve the projected energy efficiency benefits, a desired tunneling current (I_{on}) at the device on-state, a high on-off current ratio (I_{on}/I_{OFF}) and an average steep SS over a few decades of current change are the key design factors for TFETs. Among the various approaches towards the optimal TFET designs, GaSb-InAs hetero-junction tunnel FETs (HTFETs) (Fig. 3) exhibit promising performance with a simultaneous enhancement of the I_{on} and I_{on}/I_{OFF} ratio by taking advantages of the hetero-band alignment [7]–[11], [33].

Due to the asymmetrical source/drain of the p-i-n structure, TFETs also exhibit unique device characteristics such as unidirectional conduction, enhanced on-state Miller effects, and gated negative differential resistance (NDR) characteristic in the forward biased p-i-n diode regions [20]. These characteristics have strong impacts on the circuit and system designs, which require certain modifications of the circuit topologies (e.g., TFET SRAMs, pass-transistor logic, etc., [14]) to ensure their operations and performance benefits. Some of the characteristics, such as gated NDR, have been further explored to achieve more functionality in system designs [29].

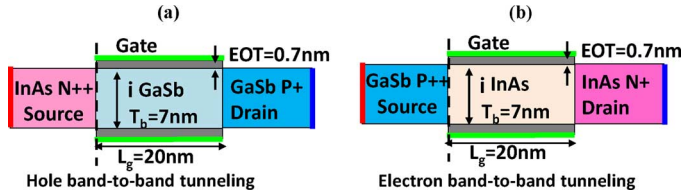

Fig. 3. Device schematics of double-gate (a) III-V P-HTFET and (b) III-V H-HTFET with 7 nm ultra-thin body T_b, 20 nm gate-length L_g, and 0.7 nm effective oxide thickness (EOT).

In addition to the digital applications, TFETs also exhibit preferred device characteristics for ultra-low power analog/RF applications. Desired high-frequency performance and significant power reduction with channel-length scaling have recently been reported in the fabricated near broken-gap III-V HTFETs [11]. Authors in [19] have first employed the high g_m/I_{DS} characteristic of the SiGe TFET beyond the MOSFET theoretical limit of 40 V^{-1} to achieve nanowatt power consumption in an operational transconductance amplifier (OTA) design. Our previous work in [21] has examined the low turn-on voltage and uni-directional conduction characteristics of the III-V HTFET in a 4-T cross-coupled rectifier design, showing its device advantages to improve the PCE and communication ranges for UHF RFID applications. In [21], the time-dependence of the power losses and the increase of the leakage power at a large RF input signal were not considered resulting in the overestimation of PCE. In contrast to [21], we include these losses in our evaluations. Also, since we have assumed a pseudo P-HTFET with symmetrical drive strength as the N-HTFET, the potential performance degradation of III-V P-HTFET has not been included in [21]. In this work, we adopt the III-V P-HTFET model generated from TCAD simulation taking into account of its degraded drive current and SS. We extend our evaluations on different HTFET rectifier topologies to further explore its device advantages compared to Si FinFET rectifier. The performance evaluations and optimizations are based on the detailed examinations of the design parameters to seek for the optimal sensitivity with a high PCE.

B. The TFET Technology Modeling

GaSb-InAs HTFETs exhibit desired I_{on} and steep SS among various TFET designs (Section III-A), which are used in our evaluations. In order to perform the circuit simulation, a look-up table based Verilog-A model [14] developed from the TCAD Sentaurus device simulation [30] has been applied for HTFET rectifier circuit design using Spectre [31]. In the TCAD simulations, the double-gate n-type GaSb-InAs HTFET device model has been calibrated with full-band atomistic simulations in [14], [28] to account accurately for the inter-band tunneling transitions [Fig. 3(a)]. The corresponding p-type III-V HTFET [Fig. 3(b)] has been generated from TCAD device simulation. This model is more realistic than [21] which assumed the symmetrical drive strength for P-HTFET and N-HTFET. A double-gate Si FinFET model is used for baseline comparisons,

TABLE I
MODEL PARAMETERS

	N-HTFET	P-HTFET	Si FinFET
Gate length (L_g)	20 nm	20 nm	20 nm
EOT (HfO_2)	0.7 nm	0.5 nm	0.7 nm
Body thickness (T_b)	7 nm	0.7 nm	10 nm
Source doping concentration	4×10^{19} cm^{-3}	5×10^{18} cm^{-3}	1×10^{20} cm^{-3}
Drain doping Concentration	2×10^{17} cm^{-3}	5×10^{19} cm^{-3}	1×10^{20} cm^{-3}
Gate work-function	4.85 eV	4.285 eV	4.55 eV
Hetero-junction band alignment	$E_{g,GaSb}$=0.845 eV, $E_{g,InAs}$=0.49 eV, ΔE_c=0.439eV		–

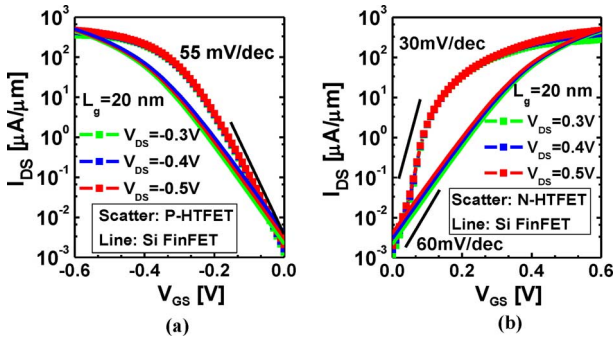

Fig. 4. Device characteristics of (a) P-HTFET I_{DS}-V_{GS} (b) N-HTFET I_{DS}-V_{GS} at different V_{DS}, and (c) on-state channel resistance R_{on} compared to Si FinFETs.

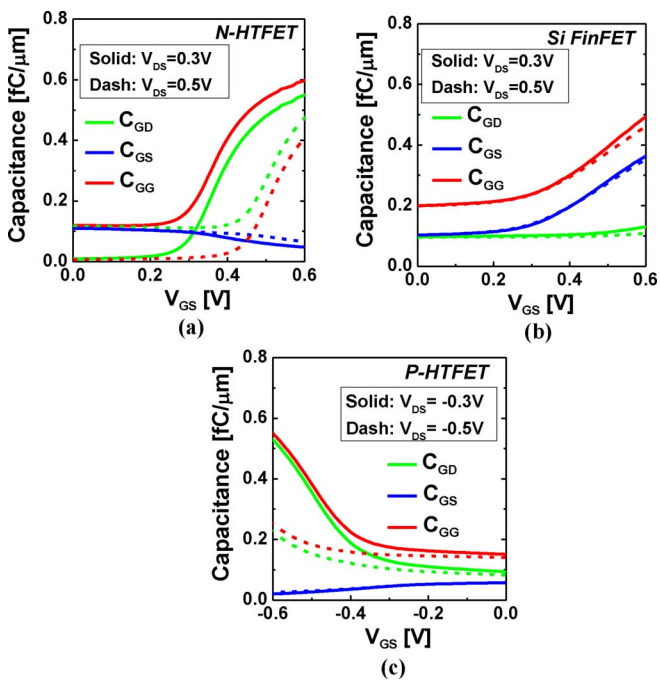

Fig. 5. Capacitance characteristics of C_{GG}, C_{GS}, C_{GD} for (a) N-HTFET, (b) Si FinFET, (c) P-HTFET at $V_{DS} = 0.3$ V and 0.5 V.

which has been calibrated to the experiment data in [30]. Symmetrical drive strength is assumed for p-type Si FinFET.

Table I shows the detailed parameters in TCAD simulation. Figs. 4 and 5 show the device characteristics, including the dc current characteristics, on-state channel resistance as well as the capacitance characteristics. At $V_{DD} = 0.3$ V, $I_{OFF} = 2$ nA/μm, the N-HTFET with a 20 nm gate-length L_g shows 7 times I_{on} improvement over the baseline Si FinFET. An average SS of 30 mV/decade over two current decades is achieved in N-HTFET, whereas the P-HTFET exhibits a degraded SS of 55 mV/decade. HTFETs also exhibit enhanced on-state Miller capacitance effect [44], [45] where the gate-drain capacitance C_{GD} dominates the total capacitance C_{GG} as opposite to the Si FinFET case (C_{GS} dominates). But due to the reduced density of states in III-V materials, the total capacitance C_{GG} is relatively lower than Si FinFET at $V_{GS} = V_{DS} = V_{DD}$ [18].

In the Verilog-A models, device characteristics of $I_{DS}(V_{GS}, V_{DS})$, $C_{GS}(V_{GS}, V_{DS})$, and $C_{GD}(V_{GS}, V_{DS})$ across a range of V_{DS} and V_{GS} are included in the models. Therefore, both dc and ac characteristics are captured in the circuit simulation.

C. TFET Advantages for RF Rectifier Design

In an RF rectifier design, the dc output power ($P_{dc,out}$), dc output voltage ($V_{dc,out}$) and power conversion efficiency (PCE) are the key performance metrics. At a given input RF power $P_{RF,in}$ with an rms voltage amplitude of V_{ac} and a load resistance R_L, $V_{dc,out}$ and PCE of a rectifier are expressed as

$$V_{dc,out} = 2V_{ac} - V_{Drop} \tag{1}$$

$$PCE = \frac{P_{dc,out}}{P_{RF,in}} = \frac{I_{dc,out}V_{dc,out}}{\frac{1}{T}\int_0^T I_{ac,in}(t)dt} = \frac{P_{dc,out}}{P_{dc,out} + P_{Loss}} \tag{2}$$

$$P_{Loss} = P_{Leakage} + P_{Reverse} + P_{Switching} + P_{Redistribute} + P_{Resistive} \tag{3}$$

where P_{Loss} represents the average power loss in the rectifier, including the transistor off-state leakage loss $P_{Leakage}$, the average capacitive switching loss $P_{Switching}$ due to the discharge of the parasitic capacitance during switching, the reverse conduction loss $P_{Reverse}$ due to the current that flows from the output node back to the input with nonfully-closed transistors under a sinusoid signal input, the power loss $P_{Redistribute}$ due to the charge redistribution between the coupling capacitors and the transistor network, and the resistive power loss $P_{Resistive}$ due to nonzero transistor on-state channel resistance R_{on} [21], [24], [46]. V_{Drop} is the lumped voltage loss across the rectifier circuit. In order to achieve a high PCE at a given $P_{RF,in}$, minimizing these power losses is critical. The HTFET device characteristics such as steep slope, high on-state current at low supply voltages and uni-directional conduction can be employed to reduce the power losses in the rectifier design.

1) Turn-On Voltage Reduction: As shown in Fig. 6(a), the steep SS characteristic of HTFET leads to the effectively low turn-on voltage as compared to Si FinFETs at the same off-state current. Such a low turn-on voltage extends the utilization range of weak RF signals, and hence improves the rectifier sensitivity without increasing the leakage power. This advantage of HTFETs relaxes the tradeoff between the turn-on voltage and leakage power as in a CMOS rectifier. Consequently, a high

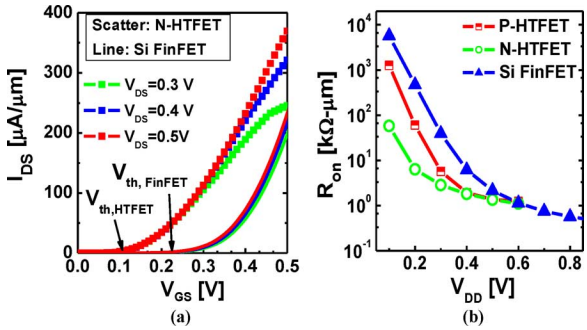

Fig. 6. (a) Linear plots of the I_{DS}-V_{GS} characteristics of the N-HTFET and Si FinFET to illustrate the turn-on voltages of the devices. (c) On-state channel resistance R_{on} comparing N-HTFETs, P-HTFET, and Si FinFETs.

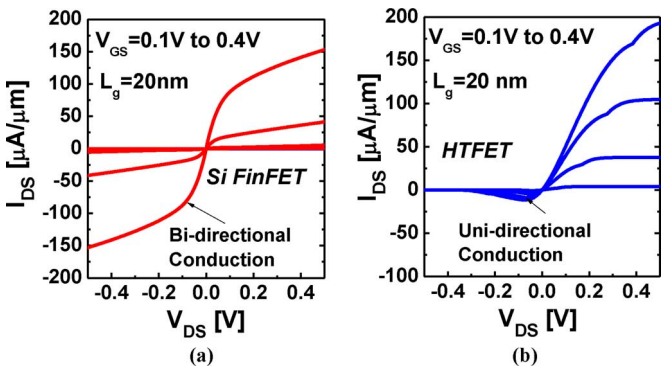

Fig. 7. (a) Si FinFET I_{DS}-V_{DS} characteristics showing bi-directional conduction. (b) N-HTFET I_{DS}-V_{DS} characteristics showing uni-directional conduction.

PCE at a low RF input power (improved sensitivity) is achievable in the HTFET rectifier.

2) On-State Resistance Reduction: As discussed in Section II-B, the reduced current of Si FinFET in subthreshold or near threshold regime results in a large on-state channel resistance with an increased power loss ($P_{Resistive}$) and V_{Drop}, which degrades both PCE and $V_{dc,out}$ [(2)]. Compared to Si FinFETs, III-V HTFETs exhibit high on-current at low supply voltages [Fig. 4(a) and (b)]. As shown in Fig. 6(b), a significant reduction of on-channel resistance can be achieved in HTFETs, which reduces the resistive power loss $P_{Resistive}$, and thereby improves the PCE at low input voltages.

3) Reverse Leakage Reduction: With the ambipolar transport suppression, the asymmetrical source/drain design of HTFETs leads to uni-directional conduction shown in Fig. 7(b), as opposed to the bi-directional conduction characteristic in Si FinFETs [Fig. 7(a)]. This unique device property of HTFET reduces the reverse conduction induced power loss $P_{Reverse}$ and further improves the PCE.

IV. TFET RF Rectifier Topologies

Based on the theoretical analysis and simulation setup, we evaluate the HTFET rectifier designs using the following three topologies: 2-T SVC (H2T) and 4-T cross-coupled (H4T) designs using both n-type and p-type HTFETs, and the 4-T N-HTFET-only design (H4N). The H4N design takes into account of the performance advantages of the III-V N-HTFET

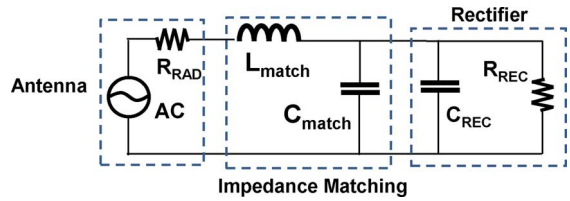

Fig. 8. Equivalent circuits of the rectifier with impedance matching network.

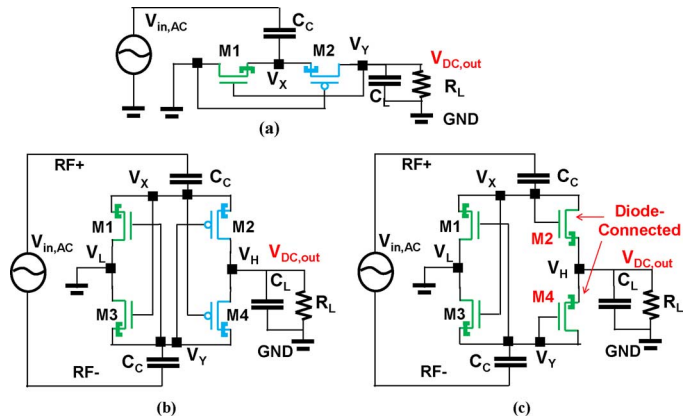

Fig. 9. HTFET RF rectifier topologies: (a) H2T, (b) H4T, and (c) H4N.

compared to the III-V P-HTFET in terms of the on-current and the steepness of SS. The orientation of HTFET is carefully examined due to its uni-directional current characteristic. To justify the performance benefits of the HTFET rectifiers, we use the 4-T cross-coupled Si FinFET rectifier (F4T) as the baseline design, A classical ideal *L-C* impedance matching network shown in Fig. 8 is applied to maximize the power delivery to the following circuitry.

A. H2T

Fig. 9(a) shows the H2T SVC rectifier using HTFETs which employs the corresponding CMOS design in [23]. This topology is derived from the conventional diode-connected rectifier, except that it uses the dc output voltage $V_{dc,out}$ to statically "cancel" the threshold voltages of the transistors. The gates of N-HTFET M1 and P-HTFET M2 are statically biased to the $V_{dc,out}$ and the ground, respectively. During the negative half of the cycle (when the input voltage amplitude $V_{RF,in} < 0$ V), M1 switches on as $V_{GS,M1} = V_{dc,out} + |V_{RF,in}| > V_{th,M1}$ ($V_{th,M1}$ is the turn-on voltage of the M1), while M2 is off. The current flows from V_Y to V_X through the load resistor R_L and the virtual ground. Similar operation is applied to the positive half of the cycle for P-HTFET switching-on. Compared to the diode-connected rectifier design, this static bias boosts the V_{GS} of the transistors with $|V_{dc,out}|$ to improve the sensitivity of the weak incoming RF signal, which also effectively reduces the on-state channel resistance R_{on} power loss accordingly. Note that with the same input voltage amplitude $V_{RF,in}$, the H2T rectifier has a larger $V_{dc,out}$ than the designs using the differential-drive signals (e.g., the H4T rectifiers). A main drawback in this design is the static voltage bias remains at the transistor off-state, causing an increase of the leakage current and the power loss and hence a relatively low PCE.

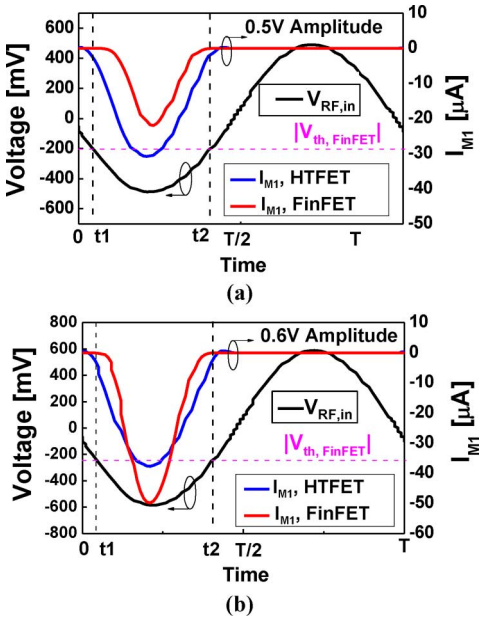

Fig. 10. Waveforms of voltage and M1 drain-source current in H4T and F4T rectifiers at (a) 0.5 V and (b) 0.6 V input voltage amplitudes.

B. H4T

Fig. 9(b) shows the H4T rectifier derived from the standard cross-coupled CMOS rectifier with the dynamic threshold voltage "cancelation" technique [24]. A differential input signal $\mathrm{V_{RF,in}}$ is applied across nodes RF+ and RF−, whereas a dc output voltage $\mathrm{V_{out,dc}} = \mathrm{V_H}$ develops across the load $\mathrm{R_L}$. When (RF + −RF−) increases beyond the transistor threshold $\mathrm{V_{th}}$ during the positive half of the input cycle, P-HTFET M2 and N-HTFET M3 switch on, resulting in current flowing into the load RL, while N-HTFET M1 and P-HTFET M4 remain off. Continuing through the cycle as (RF + −RF−) drops below the transistor threshold, M2 and M3 turn off while M1 and M4 are still off. Until (RF + −RF−) becomes more negative than $-|\mathrm{V_{th}}|$, M1 and M4 switch on to rectify the negative half of the RF signal. The dynamic threshold voltage "cancellation" is realized with the common voltage $\mathrm{V_{cm}}$ as a dc bias developed at V_X and V_Y simultaneously: $\mathrm{V_{cm}} = (V_X + V_Y)/2 \approx \mathrm{V_{dc,out}}/2$. Taking M1 as an example, the terminal voltages can be expressed as

$$\mathrm{V_{G,M1}} = V_Y = \mathrm{V_{cm}} - 0.5\mathrm{V_{RF,in}} \quad (4)$$

$$\mathrm{V_{S,M1}} = V_X = \mathrm{V_{cm}} + 0.5\mathrm{V_{RF,in}} \quad (5)$$

$$\mathrm{V_{GS,M1}} = V_Y - V_X = -\mathrm{V_{RF,in}} \quad (6)$$

$$\mathrm{V_{DS,M1}} = -V_X = -0.5\mathrm{V_{RF,in}} = 0.5\mathrm{V_{GS,M1}}. \quad (7)$$

To further illustrate the rectifier operation, we evaluate the M1 operation during a single signal cycle from $[0, \mathrm{T}]$ for both HTFET and Si FinFET based designs at 0.5 V and 0.6 V input signal amplitude, as shown in Fig. 10(a) and (b), respectively. With respect to the Si FinFET threshold voltage $\mathrm{V_{th,SiFinFET}}$, the M1 operation in $[0, \mathrm{T}]$ can be divided into four regions: subthreshold $[0, \mathrm{t_1}]$, on-state $[\mathrm{t_1}, \mathrm{t_2}]$, subthreshold $[\mathrm{t_2}, \mathrm{T}/2]$, and off-state $[\mathrm{T}/2, \mathrm{T}]$. These four regions are described as follows.

1) *Region* $[0, \mathrm{t_1}]$, $[\mathrm{t_2}, \mathrm{T}/2]$: when $\mathrm{V_{GS,M1}} = -\mathrm{V_{RF,in}} < \mathrm{V_{th,SiFinFET}}$

$$\mathrm{I_{M1,FinFET}} \approx \mathrm{I_{OFF,FinFET}} \cdot 10^{\mathrm{V_{GS,M1}}/SS_{\mathrm{FinFET}}} \quad (8)$$

$$\mathrm{I_{M1,HTFET}} \approx \mathrm{I_{OFF,HTFET}} \cdot 10^{\mathrm{V_{GS,M1}}/SS_{\mathrm{HTFET}}} \quad (9)$$

where $\mathrm{I_{OFF,FinFET}}$ and $\mathrm{I_{OFF,HTFET}}$ are the zero-bias off-state current of Si FinFET and HTFET, respectively. Since the SS of Si FinFET $SS_{FinFET} > 60\,\mathrm{mV/decade}$, and the average of SS of HTFET $\mathrm{SS_{HTFET}} = 30\,\mathrm{mV/decade}$, we have $\mathrm{I_{M1,HTFET}} > \mathrm{I_{M1,SiFinFET}}$ in $[0, \mathrm{t_1}]$ and $[\mathrm{t_2}, \mathrm{T}/2]$.

2) *Region* $[\mathrm{t_1}, \mathrm{t_2}]$: when $\mathrm{V_{GS,M1}} = -\mathrm{V_{RF,in}} > \mathrm{V_{th,SiFinFET}}$

$$\mathrm{I_{M1,Si\ FinFET}} < \mathrm{I_{M1,HTFET}} \text{ when } |\mathrm{V_{RF,in}}| < 0.5\ \mathrm{V} \quad (10)$$

$$\mathrm{I_{M1,Si\ FinFET}} > \mathrm{I_{M1,HTFET}} \text{ when } |\mathrm{V_{RF,in}}| > 0.5\ \mathrm{V}. \quad (11)$$

Since HTFET exhibits higher current for an input RF signal amplitude below 0.5 V, improved $V_{\mathrm{dc,out}}$ and PCE can be achieved simultaneously in HTFET rectifier (Section III-C). Recent research reveals that the TFET current driving ability above 0.6 V could be improved by reducing the gate-dielectric, body-thickness, or the tunneling barrier [20], [28].

3) *Region* $[\mathrm{T}/2, \mathrm{T}]$: when $\mathrm{V_{GS,M1}} < 0$ in $[\mathrm{T}/2, \mathrm{T}]$, ideally M1 is off with only leakage power loss caused by $\mathrm{I_{OFF}}$. According to (4) and (5), $\mathrm{V_{cm}}$ is developed as $\mathrm{V_{dc,out}}$ is formed, resulting in a reverse conduction of Si FinFET due to its symmetrical source/drain design [24], [26]. In the H4T rectifier, this reverse conduction can be eliminated owning to its uni-directional conduction characteristics.

The operation analysis of the 4-T cross-coupled rectifier further illustrates the significant advantages of HTFET rectifier over the Si FinFET designs for achieving higher PCE at low RF input signals with improved sensitivity and operation ranges.

C. H4N

Given the existing challenges of p-type III-V HTFET development [33] and the degraded SS of P-HTFET, we propose an N-HTFET-only RF rectifier by replacing the P-HTFETs with the diode-connected N-HTFETs, as shown in Fig. 9(c). Such an N-HTFET-only design potentially further improves the performance of the H4T rectifier. The operation of the H4N rectifier is similar as the H4T rectifier, except that the rectifying operation of the P-HTFET in H4T design is completed by the diode-connected N-HTFET. Benefiting from its steep SS characteristics, the reduced turn-on voltage of the N-HTFET also contributes to a smaller turn-on voltage of the diode-connected N-HTFETs and higher sensitivity than the rectifiers using conventional diode-connected MOSFETs.

V. Performance Evaluation and Design Optimizations

In this section, we present performance evaluation including dc output voltage $V_{\mathrm{dc,out}}$ and PCE with regards to the input

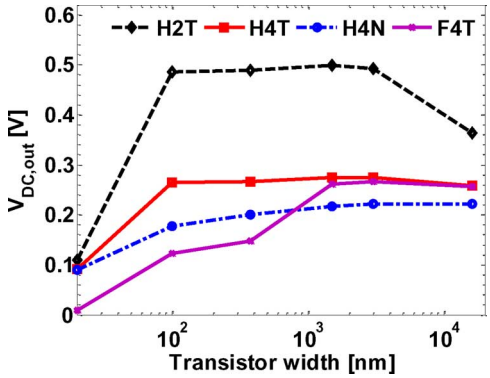

Fig. 11. $\mathrm{V_{dc,out}}$ versus W at 0.30 V input amplitude with $\mathrm{C_C} = 1.0$ pF, $\mathrm{R_L} = 1.0$ MΩ.

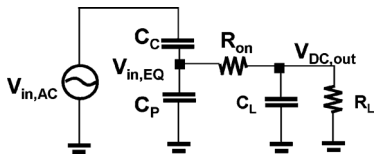

Fig. 12. Capacitive divider model with the rectifier transistor capacitance $\mathrm{C_P}$.

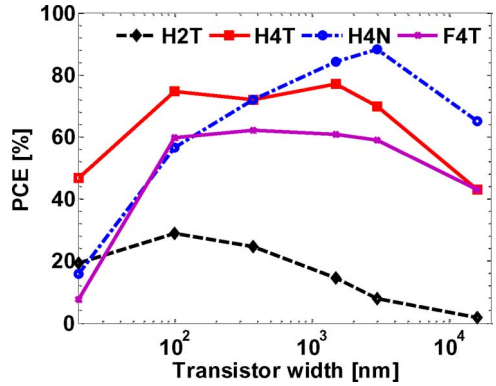

Fig. 13. Peak PCE versus the transistor width with $\mathrm{C_C} = 1.0$ pF, $\mathrm{R_L} = 1.0$ MΩ.

RF power level for different HTFET rectifier designs, and compare with the baseline F4T Si FinFET rectifier design discussed in Section IV. We focus on examining the design parameters including transistor sizing, coupling capacitance, and their impacts on the peak PCE, $\mathrm{V_{dc,out}}$ to seek for the optimal PCE and sensitivity range for energy harvesting applications.

In the following simulations, the load resistance $\mathrm{R_L}$ is set to be 1.0 MΩ, unless specified otherwise. In addition, the load capacitance $\mathrm{C_L}$ is set to be the same as the input coupling capacitance $\mathrm{C_C}$ for simulation simplicity.

A. Transistor Sizing and Coupling Capacitance Optimizations

The transistor sizing has a strong impact on both the $\mathrm{V_{dc,out}}$ and the PCE. The main tradeoff exists between a resistive power loss $\mathrm{P_{Resistive}}$ due to nonzero on-state channel resistance R_{on} (decreases with transistor width W) and the other power losses in (3) due to the transistor capacitance (increases with W). Fig. 11 shows the simulated $\mathrm{V_{dc,out}}$ at 0.3 V input versus W for H2T, H4T, H4N, and F4T designs. When W increases, less $\mathrm{R_{on}}$ results in a higher $\mathrm{V_{dc,out}}$ with less $\mathrm{V_{Drop}}$, until the transistor capacitance is prominent which limits the equivalent input voltage $\mathrm{V_{IN,EQ}}$. As illustrated in Fig. 12, the equivalent total transistor capacitance C_P forms as an ac voltage divider in series with the input coupling capacitance $\mathrm{C_C}$, and affects $\mathrm{V_{IN,EQ}}$ in the ways of

$$V_{\mathrm{IN,EQ}} = \mathrm{V_{RF,in}} \times \frac{(\mathrm{j}\omega \mathrm{C_P})^{-1} \| \mathrm{Z_L}}{(\mathrm{j}\omega \mathrm{C_C})^{-1} + (\mathrm{j}\omega \mathrm{C_P})^{-1} \| \mathrm{Z_L}} \tag{12}$$

where

$$\mathrm{Z_L} = \mathrm{R_{on}} + \mathrm{R_L} \| (\mathrm{j}\omega \mathrm{C_L})^{-1}. \tag{13}$$

As a result, a large W results in excessive $\mathrm{C_P}$, which can lower the $\mathrm{V_{IN,EQ}}$ of the rectifier.

Fig. 13 shows the impact of W on the PCE. Each point in the PCE curves represents the peak PCE with different RF input power to obtain the optimized transistor width $\mathrm{W_{OPT}}$ where the highest PCE occurs. For example, when W is smaller than $\mathrm{W_{OPT}}$, $\mathrm{P_{Resistive}}$ dominates; and when W is larger than $\mathrm{W_{OPT}}$, the other power losses in (3) increase and degrade the PCE. As shown in Fig. 13, the optimum $\mathrm{W_{OPT}}$ for the H4T rectifier is smaller than of the H4N rectifier. This is mainly because (1) the H4N rectifier needs a larger transistor W than that of the H4T rectifier to reduce the $\mathrm{V_{DROP}}$ across the diode-connected N-HTFETs, and (2) the diode-connected N-HTFET has less capacitance than the transistor connected N-HTFET arising from the dominant $\mathrm{C_{GD}}$ in HTFET (Section III-C). When shorting the gate and the drain terminals, $\mathrm{C_{GD}} = 0$ reduces the total capacitance, leading to less $\mathrm{P_{Switching}}$ and $\mathrm{P_{Resistribute}}$. This allows us to choose a larger transistor size in the H4N rectifier design to compensate the increased $\mathrm{P_{Resistive}}$ from the diode-connected transistor and achieve a comparable PCE with H4T designs at low RF input power.

Figs. 14 and 15 illustrate the $\mathrm{V_{dc,out}}$ and PCE dependence on the coupling capacitance $\mathrm{C_C}$, respectively. The impact of $\mathrm{C_C}$ on the rectifier can also be related to (12). When $\mathrm{C_C}$ is small, $\mathrm{V_{IN,EQ}}$ decreases resulting in a low $\mathrm{V_{dc,out}}$ and PCE. On the other hand, when the $\mathrm{P_{redistribute}}$ becomes dominant as $\mathrm{C_C}$ increases both $\mathrm{V_{dc,out}}$ and PCE decrease which degrade the performance. This analysis agrees with the simulation results in Figs. 14 and 15 for all evaluated topologies. Note that at a given $\mathrm{V_{RF,in}}$, the H2T rectifier design exhibits a relatively large $\mathrm{V_{dc,out}}$ and a degraded PCE compared to the other 4-T designs, which is expected as discussed in Section IV-A.

Given that the H4N rectifier has two diode-connected N-HTFETs, the transistor size of the diode-connected and transistor-connected N-HTFETs should be optimized simultaneously to obtain the highest PCE. Fig. 16 illustrates the maximum PCE when varying the width of the diode-connected N-HTFET ($\mathrm{W_D}$) in the H4N rectifier. Hence, a $\mathrm{W_T/W_D}$ ratio of 1.5 μW/4 μm is applied for the optimal performance.

Based on the evaluations of the transistor sizing and coupling capacitance effects, we use the following design parameters for each rectifier topology for optimized performance: For H2T, $\mathrm{C_C} = 0.2$ pF, $\mathrm{W} = 0.5$ μm. For H4T, $\mathrm{C_C} = 1.28$ pF, $\mathrm{W} = 5$ μm; For H4N, $\mathrm{C_C} = 2.56$ pF, $\mathrm{W_T} = 15$ μm, $\mathrm{W_D} = 40$ μm;

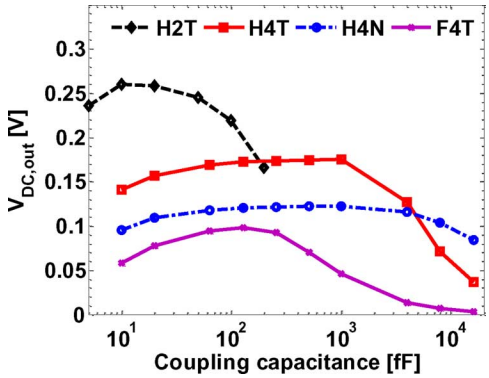

Fig. 14. $V_{dc,out}$ versus C_C at 0.20 V input amplitude with 1.0 MΩ R_L, 60 nm transistor width for H2T, and 1.5 μm transistor size for others.

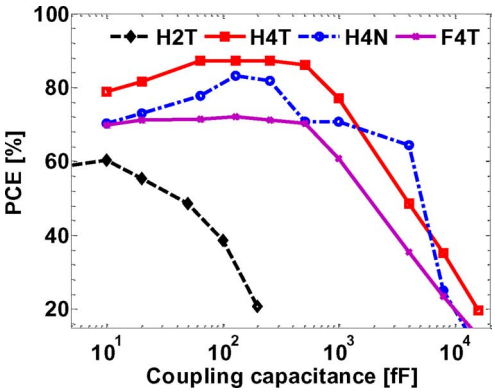

Fig. 15. Peak PCE versus C_C with 1.0 MΩ R_L, 60 nm transistor width for H2T, and 1.5 μm transistor width for others.

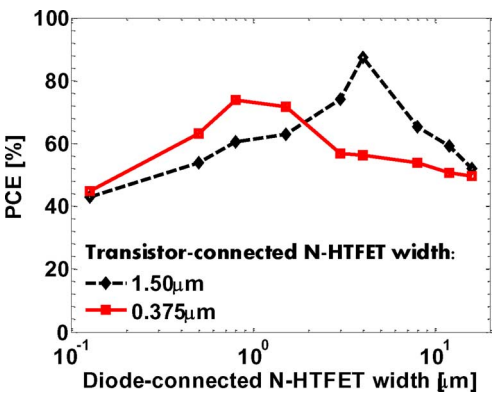

Fig. 16. Peak H4N PCE versus W_D with $C_C = 1.0$ pF and $R_L = 1.0$ MΩ.

For F4T, $C_C = 5.12$ pF, W = 5 μm. $R_L = 100$ kΩ is used in the following evaluations.

B. Single-Stage DC Output Voltage and PCE Comparisons

The $V_{dc,out}$ and PCE comparisons between the optimized rectifiers with different topologies are shown in Figs. 17 and 18 (with $R_L = 100$ kΩ), respectively. When the input power $P_{RF,in}$ is lower than −30 dBm, the H4T and H4N rectifiers show higher $V_{dc,out}$ than the F4T rectifier. As $P_{RF,in}$ increases, a cross-over of the $V_{dc,out}$ occurs, where F4T rectifier shows a comparable $V_{dc,out}$ with H4T but higher than H4N. This is consistent with the analysis in Section IV. With a low $P_{RF,in}$, the

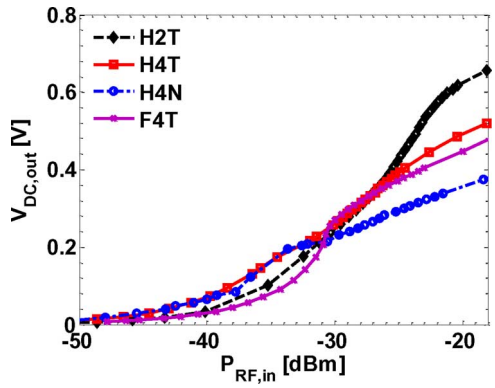

Fig. 17. $V_{dc,out}$ versus $P_{RF,in}$ for optimized single-stage rectifiers with 100 kΩ R_L.

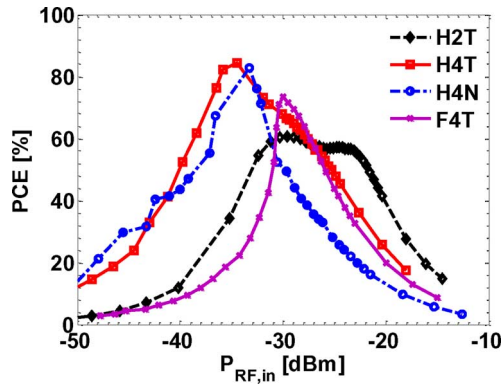

Fig. 18. PCE versus $P_{RF,in}$ for optimized single-stage rectifiers with 100 kΩ R_L.

reduced turn-on voltage and reduced R_{on} of the HTFET results in a higher $V_{dc,out}$ in the HTFET rectifier than that in the Si FinFET rectifier. As $P_{RF,in}$ increases, $V_{dc,out}$ of F4T is comparable with that of H4T and H4N due to the improved on-state current of Si FinFET at higher input voltages, but also increases the reverse conduction induced power loss. As a result, $V_{dc,out}$ of H4T is comparable or even higher than that of F4T, benefited from its uni-directional conduction. Comparing the H4T and H4N designs, the optimized H4N shows a comparable $V_{dc,out}$ at lower $P_{RF,in}$, but a lower $V_{dc,out}$ than the optimized H4T at higher $P_{RF,in}$. This result is expected given the large transistor sizing of H4N as discussed in Section V-A, which complies with our design goal of optimal PCE at a low $P_{RF,in}$.

For the H2T rectifier, a lower $V_{dc,out}$ is observed when the given $P_{RF,in}$ is low compared to the H4T and H4N rectifiers, due to the inherent leakage power loss from the static gate-bias. As $P_{RF,in}$ increases to above −25 dBm, H2T rectifier shows a substantial increase of $V_{dc,out}$ compared to the others. This is because of the power loss reductions (including $P_{Switching}$ and $P_{Redistribute}$) benefited from less and smaller transistors. At a high $P_{RF,in}$, the $P_{Resistive}$ contribution is reduced due to the increased $V_{RF,in}$, while the other power losses [see (3)] become dominant. Thus, the reduced power losses in the optimized H2T rectifier leads to a higher $V_{dc,out}$ for H2T in the high $P_{RF,in}$ range.

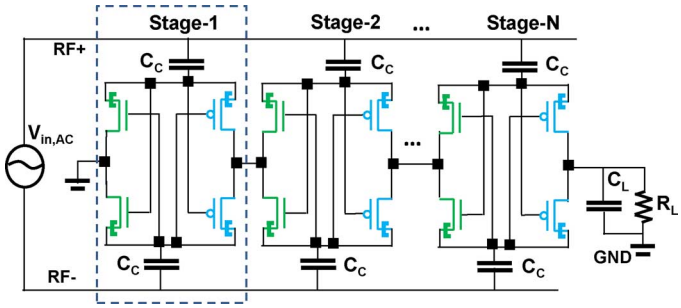

Fig. 19. Multiple-stage rectifier using H4T design as an example.

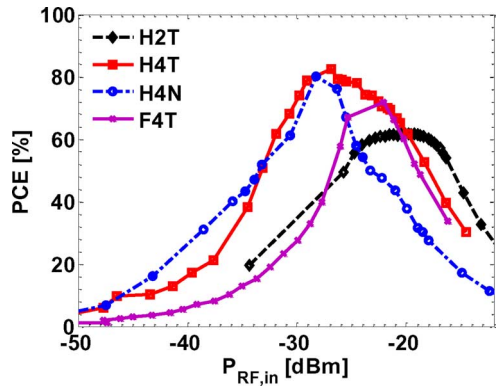

Fig. 20. PCE versus $\mathrm{P_{RF,in}}$ for two-stage optimized rectifiers with 100kΩ $\mathrm{R_L}$.

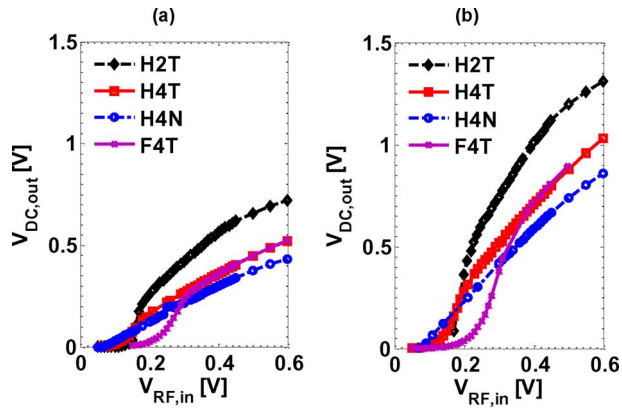

Fig. 21. $\mathrm{V_{dc,out}}$ versus $V_{RF,in}$ for single-stage and two-stage optimized rectifiers with 100 kΩ R_L. (a) Single-stage. (b) Two-stage.

Similarly to $\mathrm{V_{dc,out}}$, the PCE of the H4T and H4N rectifiers is significantly improved compared to that of the F4T rectifier, especially when $\mathrm{P_{RF,in}}$ is lower than −31 dBm (Fig. 18). For the F4T rectifier, the peak PCE of 73.5% is achieved at −30 dBm $P_{\mathrm{RF,in}}$, but drops significantly as $\mathrm{P_{RF,in}}$ approaches to the lower range. When $\mathrm{P_{RF,in}}$ is −35 dBm (0.32 μW), the PCE of the F4T rectifier drops below 21% ($\mathrm{P_{dc,out}}$ of 0.067 μW), where the H4T and H4N rectifiers reach the peak PCE of 85% and 84% ($\mathrm{P_{dc,out}}$ of 0.27 μW), respectively, which is desired for the ambient RF power harvesting applications. The H2T rectifier shows a degraded peak PCE (61%) compared to the other designs, but still outperforms the F4N at the lower $\mathrm{P_{RF,in}}$ (following the $\mathrm{V_{dc,out}}$ trend). At $\mathrm{P_{RF,in}}$ above −25 dBm, the reduced capacitive loss continues to benefit the PCE of the H2T rectifier with a highest upper $\mathrm{P_{RF,in}}$ limit to −22 dBm.

C. Multiple-Stage Design Considerations

For higher $\mathrm{V_{dc,out}}$, multiple-stage rectifiers are usually employed at the cost of PCE degradation due to extra power loss from additional stages. Fig. 19 illustrates a multiple-stage rectifier configuration using the H4T. Similar connections can be applied to the other topologies. A coupling capacitor ($\mathrm{C_C}$) is required for each stage for dc blocking. It is important to note that the input capacitance of a multiple-stage rectifier is N-times that of a single-stage rectifier, where N represents the number of stages. This is because the input coupling capacitors $\mathrm{C_C}$ of all stages are all connected to the RF input ports. As a result, the input impedance of the multi-stage rectifier strongly depends on the coupling capacitors $\mathrm{C_C}$.

Figs. 20 and 21 show the $\mathrm{V_{dc,out}}$ and PCE comparisons for the two-stage rectifiers using different topologies. The same design parameters as the optimized single-stage rectifiers in Section V-B are employed with the same $\mathrm{R_L}$ of 100 kΩ. Peak PCE of 82% and 80% are obtained in the H4T and H4N rectifiers at −27 dBm and −28 dBm $\mathrm{P_{RF,in}}$, respectively, while the 71% peak PCE is achieved in the F4T rectifier at −22 dBm $\mathrm{P_{RF,in}}$. The degraded sensitivity of the two-stage rectifier designs is due to the effective load change from the rectifier cascading. The advantage of a higher PCE for H4T and H4N preserves for the $\mathrm{P_{RF,in}}$ below −26 dBm. Benefiting from the multiple-stage connection, at $\mathrm{V_{RF,in}} = 0.3$ V, improved $\mathrm{V_{dc,out}}$ of 0.5 V, 0.43 V, and 0.75 V are achieved for the two-stage H4T, H4N, and H2T rectifiers, showing approximately 1.92×, 1.86× and 1.78× improvement than that of the single-stage cases, respectively, comparing to the 0.4 V $\mathrm{V_{dc,out}}$ with 1.6× improvement obtained for the F4T rectifier. Since the $\mathrm{V_{dc,out}}$ of the proposed two-stage HTFET rectifier with over −26 dBm $P_{\mathrm{RF,in}}$ is already higher than 0.4 V, which is sufficient for the supply voltage requirement for the HTFET circuits, multiple-stage rectifier designs with more than two stages are not discussed in this paper.

TABLE II
RF RECTIFIER PERFORMANCE SUMMARY *

Rectifier topology	F4T	H2T	H4T	H4N
Process technology	20 nm Si FinFET	20 nm HTFET	20 nm HTFET	20 nm HTFET
Transistor $V_{th,NFET}$, $V_{th,PFET}$ (V)	0.21, -0.21	0.1, -0.12	0.1, -0.12	0.1, -0.12
Single-stage $P_{RF,in}$ range (dBm) @ PCE>50%	-31 ~ -26	-33 ~ -22	-40 ~ -25	-38.5 ~ -30
2-stage $V_{DC,out}$ (V) @ $V_{RF,IN}$=0.25 V	0.13	0.61	0.41	0.32
Single-stage $P_{DC,out}$ (μW) @ $P_{RF,IN}$=-35 dBm	0.06	0.12	0.27	0.16
Single-stage peak PCE% @ $P_{RF,IN}$ (dBm)	73.5 @ -30	61 @-29.6	85 @ -34.5	84 @ -33.5
Single-stage sensitivity (dBm) PCE>50%	-31	-33	-40	-38.5

*: Data are obtained from simulations with 100 kΩ R_L at 915 MHz RF input.

Table II summarizes the performance of the proposed HTFET rectifiers, and the Si FinFET rectifier. Benefited from the reduced threshold voltages of the 20 nm technology, both Si FinFET and HTFET based designs show desired sensitivity

down to -31dBm input power with over 50% PCE, where the 4T HTFET rectifiers (H4T and H4N) exhibit even further improved the sensitivity range compared to the 4-T Si FinFET rectifier. For the single-stage designs, over 50% PCE can be achieved for H4T and H4N designs at the input RF power ranging from -40 dBm to -25 dBm and -38.5 dBm to -30 dBm , respectively, whereas the PCE of the optimized Si FinFET rectifier is less than 50% and drops fast for below -31 dBm input RF power. Although the H2T rectifier shows a degraded peak PCE of 61% compared to the other designs, a wider RF input power range from -33 dBm to -22 dBm for over 50% PCE is still achieved as compared to the F4T design. The significantly boost of the $\mathrm{V_{dc,out}}$ can be achieved using the two-stage configurations. This high PCE of the HTFET rectifiers also leads to an improved dc output power and desired dc output voltage in the low RF input power range, which is appealing to various energy harvesting applications.

VI. Conclusion

In this work, we have evaluated the performance advantages and design insights of the GaSb-InAs HTFET high-efficiency, high-sensitivity RF rectifier designs for RF-powered systems. By taking advantages of the turn-on voltage reduction and drive current improvement at low voltages enabled by the steep subthreshold slope, as well as the uni-directional conduction owning to its asymmetrical source/drain structure, HTFET exhibits superior performance advantages in terms of improving both PCE and sensitivity of the rectifiers to mitigate the technology limitations of conventional CMOS in ambient RF power scavenging. We have explored different HTFET RF rectifier topologies and design optimizations including the 2-T SVC (H2T), 4-T cross-coupled (H4T), and the 4-T N-HTFET-only (H4N) rectifier inspired from the 4-T cross-coupled topology. Evaluations of the optimized single-stage rectifiers have shown that a $> 50\%$ PCE could be achieved in the H4T rectifier with an RF input power ranging from -40 dBm to -25 dBm, while the PCE of the baseline 4-T cross-coupled FinFET rectifier drops significantly for below -31 dBm input. A maximum PCE of 84% and 85% could be achieved in the proposed H4N at -33.7 dBm input power and H4T at -34.5 dBm input power, respectively. Such superior PCE and sensitivity improvement of the HTFET rectifiers stems from optimizations based on the unique device characteristics, which highlights the steep-slope HTFET as a promising candidate in applications with RF-energy harvesting.

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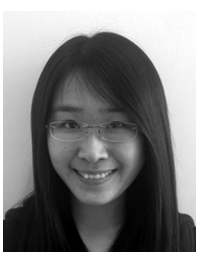

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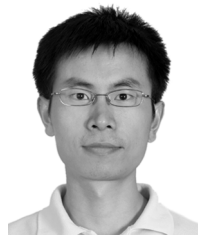

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