# Nonvolatile Processor Optimization for Ambient Energy Harvesting Scenarios

Kaisheng Ma, Xueqing Li, John Sampson
Dept. of Computer Science and Engineering
The Pennsylvania State University
State College, PA, USA
{kxm505, lixueq, Sampson}@cse.psu.edu

Yuan Xie
Department of Electrical and Computer Engineering
University of California at Santa Barbara
Santa Barbara, CA, USA
yuanxie@ece.ucsb.edu

Yongpan Liu
Dept. of Electronic Engineering
Tsinghua University
Beijing, China
ypliu@tsinghua.edu.cn

Vijaykrishnan Narayanan
Dept. of Computer Science and Engineering
The Pennsylvania State University
State College, PA, USA
vijay@cse.psu.edu

***Abstract*—Nonvolatile processors (NVPs) are emerging as a promising solution for energy harvesting scenarios, in which the available power supply is unstable and intermittent. Backup and recovery operations within NVPs can smooth the instruction operation during the power failures, even without large energy storage devices. In this work, we optimize the NVP in two aspects: (1) using emerging steep-slope tunnel FETs (TFETs) to reduce the VDD and dynamic power of the logic gates; (2) optimizing the trade-off between nonvolatile memory retention time and the memory write energy to save energy during backup operations. Simulation results prove that using TFET technology improves the forward progress by 2.7X over the CMOS LP technology, while the backup number can be reduced by an average of 38% because of less backup energy requirement.**

***Keywords- Nonvolatile processors; Energy harvesting; Tunel-FET; Retention time; Forward progress***

## I. INTRODUCTION

In energy-harvesting applications, traditional processors need a large energy storage device such as a supercapacitor to accumulate sufficient energy before a task starts. Otherwise, a task failure occurs at every power supply failure. Existing solutions to this problem are mainly the checkpoint techniques to store the intermediate computation states to external nonvolatile memory storage, e.g. flash disks, before power failures occur. However, the reset and roll-backs with communication to external data storage result in high costs of performance and power [1-5].

In contrast, nonvolatile processors (NVPs) can overcome this limitation by making use of their non-volatility feature [1-4]. An NVP is a processor with built-in nonvolatile memory (NVM) to backup the intermediate state on the chip when a power failure occurs, and restore the processor state when power comes back. With these instruction-level backup and recovery operations, the non-volatility feature is transparent to the programmers and compilers, making it compatible with more design automation techniques, and more energy-efficient than existing solutions.

Thus, being a promising candidate for energy-harvesting applications, NVPs are superior in achieving more forward progress (FP) [1-4]. To further optimize the NVP design, in this work, we propose (1) using a core structure with steep-slope tunnel FETs (TFETs) to lower the logic power, and (2) optimizing the trade-off between nonvolatile memory retention time and the memory write energy to save energy during backup operations. For the evaluation purpose, we consider the STT-RAM technology as the NVM backup option.

## II. PROPOSED OPTIMIZATION SOLUTIONS

### *A. Applying TFET to NVP logical parts*

Previous work [1] on the architecture optimization has demonstrated that, to achieve the maximum overall FP, the NVP architecture needs to adapt itself to possible high input power with a higher instruction rate even at a cost of higher energy per instruction. This is because any power more than what can be consumed is rejected or wasted by insufficient or leaky energy storage. As an out-of-order (OoO) core makes more FP with higher input power, and oppositely, a non-pipelined (NP) core better fits the low input power scenario.

On the device level, TFET, emerging as a novel steep-slope device, can be applied to NVP so as to further reduce the power and energy dissipation from NVP logical parts, such as Fetch, ALU, etc. Recently, TFETs have been very intriguing for device developers, circuit designers, and even the architecture researchers [5][6][8-11][15]. The goal of steep-slope devices is to reduce the power consumption by lowering the supply voltage for less dynamic power while keeping low leakage current and sufficient ON-current for driving capability. The <60mV/decade subthreshold slope (SS) of steep-slope devices outperforms CMOS with >60mV/decade in that further reducing CMOS power supply voltage has become challenging because of increasing leakage power.

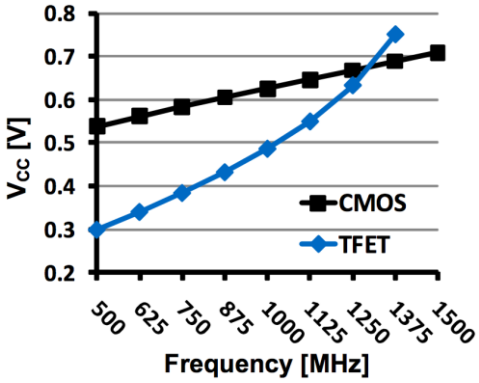
We propose the solution to apply TFET to NVP's logical parts for several reasons.

- Due to the steep-slope features, TFET cores requires much lower VDD requirement than CMOS cores with same architecture especially in low frequency region, as shown in Figure 1(a). TFET demonstrates lower VDD feature than CMOS when the frequency is lower than 1300MHz. While in the target applications with ambient energy harvesting technologies, the frequency varies from 32kHz to a few MHz, limited by the low density of ambient energy, which is far away from the 1300MHz. With this low frequency application, the TFET can sufficiently demonstrate its advantages of lower VDD.
- Lowering VDD of logic gates can reduce the energy per instruction. Assuming the income energy is a constant, a lower VDD with TFETs can reduce both the leakage and dynamic power for the core. Thus with same amount of harvested energy, TFET cores can execute more instructions than CMOS cores.
- The capability of TFET operation with a low VDD can improve the efficiency of the front-end circuit. This is because of the prevention of additional low-power-conversion-efficiency voltage boosting circuit blocks which are otherwise necessary when implementing the core in CMOS.
- While the leakage in energy storage capacitor is a significant part of the total system energy [1][2], reducing VDD can reduce the leakage of capacitor and improve the overall energy efficiency of the system.

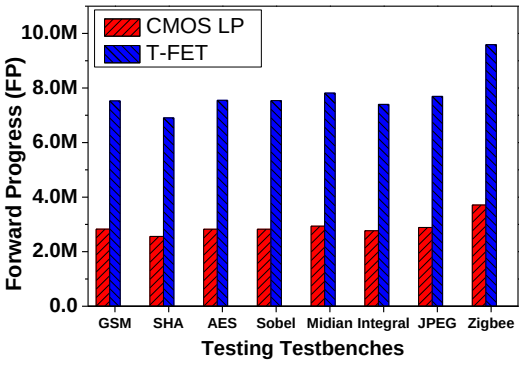
The simulation results in Fig. 1(b) confirm the FP advantage of the TFET cores compared to CMOS cores. In the simulation platform [1], a non-pipelined architecture is designed. And all the factors including front-end circuit efficiency, energy storage capacitor (470uF) leakage are taken in to consideration. As can be seen in Fig. 1(b), the forward progress of core with TFET technology can be improved by 2.7X over CMOS LP technology, with ambient RF power source.

### *B. Trade-offs between nonvolatile memory retention time and write energy*

The NVP stores the computation states in a concentrated nonvolatile memory block or distributed nonvolatile memory when a power failure occurs, and restores the states from nonvolatile memory back to computation logic when power comes back. Different power sources and scenarios can result in different backup frequency. Some vibration power sources may result in several orders more backup operations than those stable power sources like stable solar panels. No matter what power failure frequency is, the energy spent on backup and recovery operation is not desired. So it is of significance to reduce the backup energy by reducing the number of backup operations. It is also noted, that most of the backup and recovery energy is dissipated by the backup operation, because the write energy of most nonvolatile memory, including STT-RAM, PC-RAM, FeRAM, ReRAM, is much higher than the read energy [2][12-14].




(a)




(b)

Figure 1. (a) CMOS LP V.S. TFET processor operating frequency and power supply comparison, sourced from [10]. Energy harvesting scenarios can support usually frequency from 32kHz to ~MHz depending on energy sources and scenarios, so the low power supply voltage advantages that TFET exhibits are more obvious than that of CMOS. (b) By applying TFET [10-11] as volatile circuit technology with advanced dynamic power and energy management [15], the forward progress can improve 2.7X than CMOS LP technology, at ambient RF power source. The testbenches are MiBench[7].

On the other hand, if the power failure occurs more frequently, the power interval window is narrower. And accordingly, on average, the power comes back after a short time in most applications. Thus, making the nonvolatile memory retention time being as long as 10 years is not necessary. The trade-off between nonvolatile memory retention time and write energy can thus be optimized.

As for the NVP architecture, the work concentrates on the trade-off between NVM retention time and energy consumption for backup operations. Due to large amount of backup data requirement by ICache, DCache, Register Files etc. in NVP, the backup energy consumption per operation is essential. Longer NVM retention time consumes more write energy [2].

Fig. 2 in [13] and Fig. 2 in [14] show the relation between STT-RAM write current and write pulse width for different retention time. 57.6% write energy can be saved by reducing the retention time from 10 years to 1 second. By matching the retention time to the power interval profile, the write energy can be significantly reduced. But this method requires an

indicator to identify the correctness of the data. By charging a small capacitor from the main energy storage capacitor, and controlling of the leakage at this small capacitor, the power failure time can be measured. If the energy level in the small capacitor is still higher than the threshold, the NVP will restore the state and continue computing. Otherwise, NVP will reset. Fig. 2 shows 38% backup number reduction. The energy that should be used for backup when retention time is 10 years is now used for computation when retention time is 1 min.

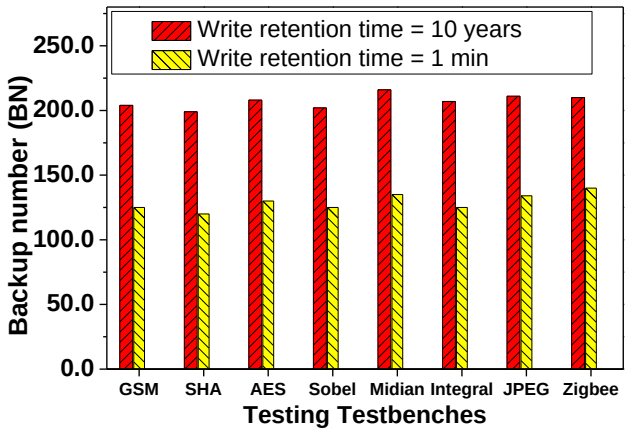



Figure 2. Ambient RF power source: Retention time reduction can reduce an average of 38% backup number count because of less backup energy requirement.

## III. Future Work

### A. *Methods for predicting the retention time*

Although reducing the retention time from 10 years to 1 minute can reduce the backup energy and backup numbers, the penalty of a wrong prediction is large: the processor needs to reset to restart all the computation.

Perfectly matching the retention time to power profile interval is almost impossible due to the uncertainty of the power income. But we can still apply some methods to maintain the system stability: CRC and Ping-Pang backup are possible options.

## IV. Conclusion

This work evaluates the NVP forward progress improvement brought by TFET technology and the optimization of the trade-off between retention time and write energy for nonvolatile backup memory .

## Acknowledgment

This work was supported in part by the Center for Low Energy Systems Technology (LEAST), sponsored by MARCO and DARPA, Shannon Lab Huawei Technologies, High-Tech Research and Development (863) Program under contract 2013AA01320, the Importation and Development of High-Caliber Talents Project of Beijing Municipal Institutions under contract YETP0102, and by the NSF awards 1160483 (ASSIST), 1205618, 1213052, 1461698, and 1500848.

## References

[1] KaiSheng Ma, et al., "Architecture exploration for ambient energy harvesting nonvolatile processors", The International Symposium on High-Performance Computer Architecture (HPCA-21). pp. 526-537. Feb. 2015.

[2] Kaisheng Ma, et al., "Nonvolatile processor architecture exploration for energy harvesting applications", IEEE Micro Special Issue on Alternative Computing Designs & Technologies. To appear.

[3] Yongpan Liu, et al. "Ambient energy harvesting nonvolatile processors: from circuit to system." Proceedings of the 52nd Annual Design Automation Conference. ACM, 2015.

[4] Yiqun Wang, et al., "A 3us wake-up time nonvolatile processor based on ferroelectric flip-flops." In ESSCIRC (ESSCIRC), 2012 Proceedings of the, pp. 149-152. IEEE, 2012.

[5] Xueqing Li, et al., "Rf-powered systems using steep-slope devices," New Circuits and Systems Conference (NEWCAS), 2014 IEEE 12th International, June 2014.

[6] Huichu Liu, et al., "Tunnel FET RF rectifier design for energy harvesting application," IEEE Journal on Emerging and Selected Topics in Circuits and Systems 2014.

[7] Guthaus, Matthew R., et al., "MiBench: A free, commercially representative embedded benchmark suite," Workload Characterization, 2001. WWC-4. 2001 IEEE International Workshop on. IEEE, 2001.

[8] U. Heo, X. Li, H. Liu, et al, "A high-efficiency switched-capacitance HTFET charge pump for low-input-voltage applications," in VLSI Design (VLSID), 2015.

[9] K. Swaminathan, H. Liu, X. Li, et al., "Steep slope devices: Enabling new architectural paradigms," Proceedings of the 51st Annual Design Automation Conference, 2014.

[10] V. Saripalli, A. Mishra, S. Datta, V. Narayanan, "An energy-efficient heterogeneous CMP based on hybrid TFET-CMOS cores," in Proceedings of the 48th Design Automation Conference. ACM, 2011.

[11] Nikonov, D.E., et al., "Overview of beyond-cmos devices and a uniform methodology for their benchmarking," Proceedings of the IEEE , vol.101, no.12, pp.2498,2533, Dec. 2013.

[12] Noguchi Hiroki, et al., "A 3.3 ns-access-time 71.2μW/MHz 1Mb embedded STT-MRAM using physically eliminated read-disturb scheme and normally-off memory architecture," In Solid-State Circuits Conference-(ISSCC), 2015 IEEE International, pp. 1-3. IEEE, 2015.

[13] Swaminathan, K., et al., "When to forget: A system-level perspective on STT-RAMs," in Design Automation Conference (ASP-DAC), 2012 17th Asia and South Pacific , vol., no., pp.311,316, Jan. 30 2012-Feb. 2 2012.

[14] Jog, A., et al., "Cache revive: Architecting volatile STT-RAM caches for enhanced performance in CMPs," Design Automation Conference (DAC), 2012 49th ACM/EDAC/IEEE , vol., no., pp.243,252, 3-7 June 2012.

[15] Huichu Liu, et al., "Tunnel FET-based ultra-low power, low-noise amplifier design for bio-signal acsquisition," in Proceedings of the 2014 international symposium on Low power electronics and design, 2014.