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Key characterization factors of accurate power modeling for FinFET circuits

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Abstract Due to its excellent device features, manufacture process compatibility and diversity of the circuit structures, The FinFET is considered appropriate candidate for the conventional bulk-MOSFET in sub-22nm technology nodes. However, the power estimation CAD tools for FinFET are missing at the moment, which mainly results from the absence of FinFET power analysis and FinFET power model. Three key factors for FinFET power model are: the dimension of the look-up-tables, that to find out the most significant factors that influence FinFET power and to make them as indexes for the look-up-tables; the distance between sampling points; and the interpolation method. In this paper, various factors that may contribute to the FinFET power consumption are evaluated. Of all the factors, the continuous ones are compared with sensitivity method. As to other discrete factors, methods of building them in power model are given according to the features of the each factor and the way it influences the power. Based on the simulation result, standard cell power library model for FinFET is proposed. The research work lays foundation for accurate power analysis and modeling for high-level power analysis of FinFET circuits. Besides, these key factors are also crucial for low-power FinFET circuit design.

Keywords FinFET, power modeling, leakage power, internal power, input slew, output load

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1 Introduction

The continuous decrease in feature size with the corresponding increase in chip density and operating frequency have made power consumption a major concern in VLSI design. Generally there are two approaches used widely in industry for power estimation. The most accurate way to calculate the cell power is to perform circuit simulation (Spice) and monitor the current waveforms between the power and ground pins. The instantaneous power can be obtained through multiplying current with the supply voltage. Thus average power and peak power for different parts of the circuit can be derived. However for digital circuits of reasonable size the simulation time is excessive, which means this method becomes unfeasible. To speed up the analysis, the power characterization of the standard cells in steady state and

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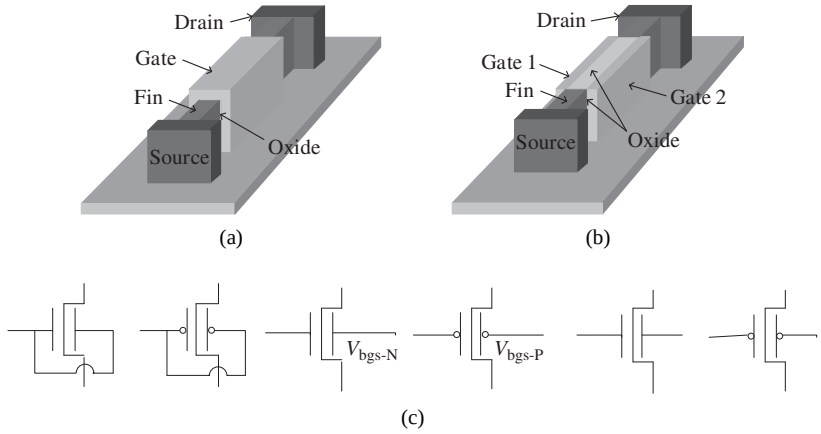

Figure 1 FinFET model and schematics. (a) Tied gate three-dimensional diagram; (b) independent gate three-dimensional diagram; (c) electrical model schematics ($V_{\text{bgs-N}}$ is Low Bias, $V_{\text{bgs-P}}$ is High Bias).

in presence of switching events is captured in the power library model [1–3]. It is required for EDA tools to estimate power consumption based on the power library model such as CCS power model [4] proposed by Synopsys and ECSM power model [5] proposed by Cadence. However the accuracy of power estimation is still unsatisfactory due to the lack of accurate power model and efficient estimation approach.

With the development of devices, FinFET, like a multi-gate transistor on SOI substrate, shows its advantages and is considered as a feasible choice for conventional MOS [6,7]. Figure 1 (a) and (b) illustrates the three-dimensional diagrams of a shorted-gate and independent-gate FinFET transistors respectively. The thin vertical silicon fin is the conductive channel and the poly-Si gate wraps the fin to control the channel effectively. Due to this multi-gate structure, FinFET devices lesson the Short Channel Effects (SCEs) and offer higher on-state current, lower off-state current and high switching speed [8].

It is noteworthy that the two vertical gate of FinFET can be separated by depositing oxide on the top of silicon fin to get two independent gates, which offers three different operating modes for FinFET devices [9]. Figure 1(c) shows the electrical schematics of three operating modes.

Shorted gate (SG): the two gates are tied together as a single gate and FinFET is regarded as a three-terminal device. This mode provides strong gate control, so that the transistor can work in the high-performance state, including high on-state current and high switching speed.

Independent gate (IG): in this mode, the two independent gates are connected to different gate voltages. The device is similar to two parallel transistors.

Low power (LP): LP mode is a special IG mode. The two gates are divided into front gate (FG) and back gate (BG). The FG connects to gate voltage, while the BG connects to bias voltage. We can change the FG threshold voltage (V_{thfg}) by adjusting the bias voltage (V_{bgs}). The relation can be expressed as follows [10,11]:

$$\frac{\delta V_{\text{thfg}}}{\delta V_{\text{bgs}}} = -\frac{C_{\text{oxb}} C_{\text{si}}}{C_{\text{oxf}}(C_{\text{oxb}} + C_{\text{si}})} \propto \frac{t_{\text{ox}}}{t_{\text{si}}}, \tag{1}$$

where C_{si}, C_{oxf}, C_{oxb}, t_{ox}, t_{si} are the body capacitance, FG capacitance, BG capacitance, oxide thickness and fin thickness, respectively. According to the above expression, if the reverse bias voltage increases, the threshold voltage will follow the trend. Thus the power consumption will decrease due to the direct correlation between leakage current and threshold voltage.

In order to support FinFET VLSI design and power analysis, it is imperative to perform research on power library model of FinFET standard cells. Compared with conventional bulk-MOSFET, FinFET has some innovative features in device structure and circuits, thus more influence factors should be considered in FinFET power library model for accurate power analysis. In this paper, the most important factors, including traditional input slew and output load, and factors that contribute to the power consumption but not yet being considered in power characterization and modeling such as input state and previous state, back-gate voltage of FinFETs, are explored and analyzed. Moreover, different sensitive degree

of these influencing factors to leakage power and internal power are discussed and new FinFET power library model is proposed.

2 Power modeling

A circuit typically dissipates a certain amount of power even without switching activity [12]. The total power consumption is sum of the leakage and dynamic power contributions [13], shown in (2). Dynamic power can be split into two components, shown in (3): the switching component associated with charging and discharging the output load C_i, shown in (4); the remaining internal component corresponds to the short-circuit power and the internal switching power. In the following equations, VDD is supply voltage and C_i is load capacitance of node i.

$$P = P_{\text{leakage}} + P_{\text{dynamic}}, \tag{2}$$

$$P_{\text{dynamic}} = P_{\text{switching}} + P_{\text{internal}}, \tag{3}$$

$$P_{\text{switching}} = \frac{1}{2} \cdot \text{VDD}^2 \cdot \sum_{i=1}^{n} C_i. \tag{4}$$

3 Bulk-MOSFET standard cell power library model introduction

Table 1 shows a part of a power library model released by ARM Inc. All the data in the library are from Hspice simulation: in the first step, the power calculation methods are built as introduced in part 2. It is followed by stimulation of the individual power part using Hspice, with the aim of accessing the parameters of the library, for example, the leakage power at every possible situation. The last step is to capsule them in to the specifically defined library format.

When power estimation is going to be done, the power analysis engine looks up at the cells used in the circuit netlist according to the names. For example, the name of the cell in Table 1 is NAND2B_X0P5M_A12TS. Then power analysis engine fetches the necessary data in the library, interpolates the data, and calculates power consumption of the cell (combining the timing stimulation wave if available). In this process, the netlist is a must, for instance, in (4), the output load for this cell is actually the sum of input capacitance of linked next cells.

In the library details, the first part is the parameter for leakage power estimation. As you can see, the leakage power is given according to different input states. For instance, "!AN&!B" stands for the input state AN = B = 0. Condering there are four static input states of a two-input NAND, there should be "!AN&!B", "!AN&B", "AN&!B" and "AN&B", of which the later three are omitted in Table 1. What's more, the library also indicates the default leakage power: "related_pg_pin: 'VDD'; value: '0.0364940274';", in case the timing waves are unavailable.

What follows in the library are the capacitances of each pin, which are parameters for switching power calculation as in (4). According to the netlist, the output load is the summary of the pin capacitance connected to the output pin and the wire-load model as shown in Table 1. In the library, each pin is defined individually. If the timing is available, power analysis engine can choose either "fall_capacitance" or "rise_capacitance". Otherwise, it uses the default capacitance. There are 3 pins in a two-input NAND (except VDD and GND): AN, B, and Y because there may be conditions that the outputs are parallely connected, the capacitance of output Y is also necessary.

When calculating the internal power, the power analysis engine uses the 2-dimension look-up-table. By "index1" and "index2", which stands for "input_ transition_time" and "total_output_net_capacitance" respectively, the values of internal power can be accessed. In Table 1, When AN = 0, the related pin is B. The table provides the internal power when B falls. The look-up-table is 7×7.

After calculation of leakage, internal and switching power, the total power of the cell can be obtained by (2).

Table 1 SMIC LOGIC0065LL SVT Process SC12 High Performance Standard Cell Power Library Model, released by ARM Inc. This library is based on SMIC 65nm technology. This is a cooperative issue between Synopsys Inc. and ARM Inc.

```
//temperature, there are three types: best, normal, and worst
  temperature (normal);
//part of the units
  capacitive_load_unit(1, pf);
  leakage_power_unit: 1uW;
//part of the library
  power_lut_template(pwr_tin_oload_7 × 7) {
    variable_1: input_transition_time;
    variable_2: total_output_net_capacitance;
    index_1("1, 2, 3, 4, 5, 6, 7");
    index_2("1, 2, 3, 4, 5, 6, 7");
  }
  lu_table_template(tmg_ntin_7) {
    variable_1: input_net_transition;
    index_1("1, 2, 3, 4, 5, 6, 7");
  }
//one of the standarded cells
  cell(NAND2B_X0P5M_A12TS) {
    area: 2.88;
    cell_footprint: nand2b;
    leakage_power() {
      related_pg_pin: "VDD";
      when: "!AN&!B";
      value: "0.0357860882";
    }
...
    pin(AN) {
      capacitance: 0.000933223;
      direction: input;
      fall_capacitance: 0.000919675;
      input_voltage: default;
      max_transition: 0.726;
      related_ground_pin: VSS;
      related_power_pin: VDD;
      rise_capacitance: 0.00094677;
...
      internal_power() {
        related_pin: "B";
        when: ""!AN";
        fall_power(pwr_tin_oload_7 × 7) {
          index_1("x,x,x,x,x,x,x");
          index_2("x,x,x,x,x,x,x");
          values("x,x,x,x,x,x,x","x,x,x,x,x,x,x","x,x,x,x,x,x,x","x,x,x,x,x,x,x", "x,x,x,x,x,x,x",
           "x,x,x,x,x,x,x","x,x,x,x,x,x,x");
        }
...   }
```

4 Key characterization factors for FinFET

The experiment is based on PTM 32 nm FinFET model[1)], which consists of two SOI MOSFETs and capacitor coupling the gates of two MOSFETs, which and the W/L of N-FinFET is 64 nm/32 nm and the W/L of P-FinFET is 180 nm/32 nm. The supply voltage is 1 V.

1) Nanoscale Integration and Modeling (NIMO) Group at ASU, PTM: http://ptm.asu.edu/, 2005.

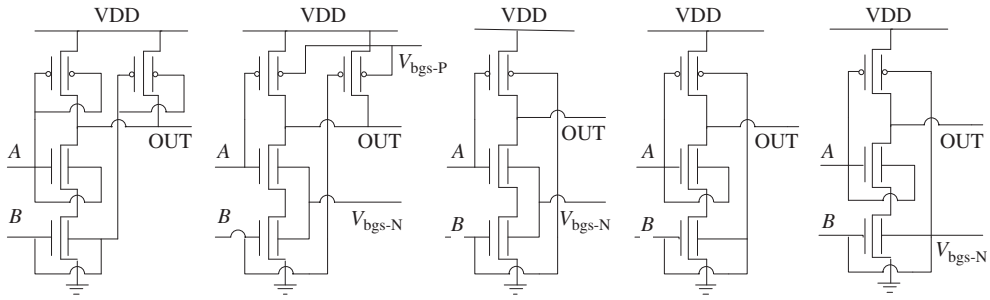

Figure 2 Five modes for FinFET two-input NAND. (a) SG-Mode; (b) LP-Mode; (c) IG/LP-Mode; (d) IG-Mode; (e) MT-Mode.

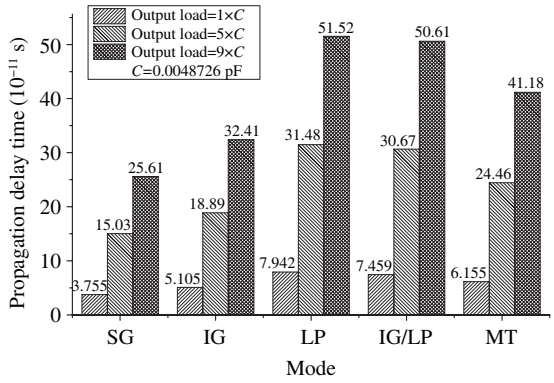

Figure 3 Mode (circuits in Figure 2) vs. propagation delay.

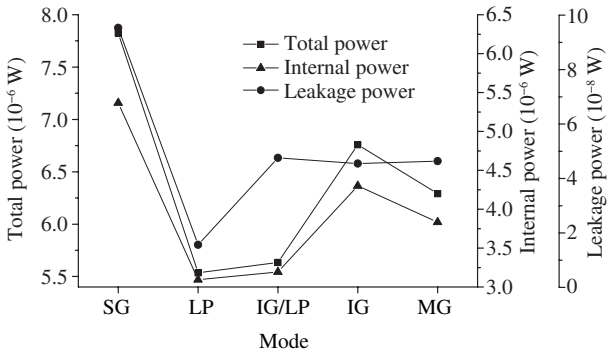

Figure 4 Mode vs. power. A two-input NAND shown in Figure 2 is tested. The input slew is 0.1 ns. The output load is 0.0048726 pF. The leakage power is tested when $A = B = 1$.

4.1 Mode

Depending on the fact that front gate and back gate of FinFET ties or not, standard cells of FinFET circuits have five different connecting modes [14], Figure 2 shows different standard cells for NAND [15]: shorted-gate mode (SG); independent-gate mode (IG); low-power mode (LP) ($V_{\text{bgs-N}}$ and $V_{\text{bgs-P}}$ are back-gate bias voltage for N-FinFETs and P-FinFETs respectively ($V_{\text{bgs-N}} = -20\% \times \text{VDD}$; $V_{\text{bgs-P}} = 120\% \times \text{VDD}$)), which derives from IG, although one of the gate is connected to a stable voltage so as to influence the threshold voltage of the other gate of FinFET; independent-gate/low-power mode (IG/LP), which is a mixed connection by using both IG and LP. This kind of connection can save area while maintaining low leakage power; mixed-terminal mode (MT), which is actually based on IG physical technology, the connection of SG in MT is through routing unlike Figure 1(a).

Figure 3 is delay comparison for different modes with different loads for NAND standard cells in which SG mode shows the best performance as it can be regarded as two parallel transistors. The propagation of LP is nearly twice of that of SG. The bias voltage connected to the back gate changes the threshold voltage of the front gate, influencing the performance. IG mode balances the area and performance. IG/LP and MT modes' delay in this cell is as bad as LP mode.

Figure 4 shows power consumption of each NAND standard cells. In the 5 mode cells, the SG one has the largest power consumption both in leakage and internal power. In LP mode, leakage power consumption is drastically reduced, to one-tenth of that of SG mode. This is because the back-gate voltage (in this test, $V_{\text{bgs-N}} = -20\% \times \text{VDD}$; $V_{\text{bgs-P}} = 120\% \times \text{VDD}$) influences the threshold voltage. The sub-threshold current is considerably reduced. The internal power of the LP mode is also much better than SG mode. These features make LP mode ideal for applications that are sensitive to power. IG mode provides abundant connection alternatives. By reducing the number of transistors in cells, the cell area can be decreased. And its power consumption is also reduced compared to SG mode. IG/LP mode combines IG and LP modes, possessing almost all the advantages of both of them except the drastic

leakage drastic reduction of LP mode. Irrespective of this, the IG/LP mode is very important because the internal power is greatly reduced compared to SG mode, and it could be seen that the unit of internal power is 10^{-6} W, while the leakage 10^{-8} W. IG/LP mode could not only reduce the area but also provide access to low power design, which is flexible. The MT mode is so flexible that it capsules all possible design methods, offering reasonable trade-off between performance power and area.

4.2 Back-gate bias voltage

Considering the gate-gate coupling of the front and back gates, threshold voltage of the front-gate varies in response to the back-gate bias voltage. A generalized model for the relationship between FinFET front gate threshold voltage and the applied back gate voltage is derived in [16]. Eq. (5) demonstrates the approximate relationship that is in consensus to present study.

$$V_{\text{thfg-N}} \approx \begin{cases} V^0_{\text{thfg-N}} - \delta \times (V_{\text{gbs-N}} - V_{\text{thbg-N}}), & \text{when } V_{\text{gbs-N}} < V_{\text{thbg-N}}, \\ V^0_{\text{thfg-N}}, & \text{otherwise}, \end{cases} \tag{5}$$

where $V_{\text{thfg-N}}$ and $V_{\text{thbg-N}}$ denote for the threshold for the N-FinFET front gate and back gate respectively, s denotes the source terminal of FinFET, δ is a positive value determined by the ratio of gate and body capacitances, and $V_{\text{thfg-N}}$ is the minimum observed $V_{\text{thfg-N}}$. Eq. (5) is for N-FinFET, but may also be applied to a P-FinFET with usual changes in sign. If the FinFET is operated in SG mode, the threshold voltages of both gates respond simultaneously to change in voltage at the other gate. As shown in (5), gate-gate coupling is observed only in the weak-inversion region of operation. In the region of strong inversion, the presence of inversion charge in the channel shields FinFET gate from each other where no coupling is observed.

In Figure 5, the back-gate voltage of N-FinFET and P-FinFET decreases and increases respectively. As a result, the front-gate threshold voltage of N-FinFET ($V_{\text{thfg-N}}$) and P-FinFET ($V_{\text{thfg-P}}$) increases and decreases respectively, which results in exponential decrease of leakage power, in contrast the circuit propagation delay increases simultaneously. In fact the internal power also varies according to back-gate voltage. As is discussed above, back-gate bias voltage is an important parameter influencing both FinFET leakage power and internal power that we must take it into consideration as one of key characterization factors.

4.3 Input slew

Input slew is used as an interpolation index of look-up-tables in bulk-silicon MOSFET power library model as introduced in Table 1. The influence of input slew to power consumption is predominantly seen in internal power. In most cases, the actual circuit is cascaded, thus the input waveform may not be ideal. In this paper, input slew is measured by choosing 30%–70% voltage in order to cut the tails the waveform, Eq. (6) is used to obtain input slew, where the T_1 is time when input is $0.7 \times$ VDD and T_2 is time when $0.3 \times$ VDD,

$$T_r = \left| \frac{T_1 - T_2}{70\% - 30\%} \right|. \tag{6}$$

In Figure 6, with the increase of input slew, the internal power of an inverter (SG and LP mode, the back-gate bias for LP: $V_{\text{bgs-N}} = -20\% \times \text{VDD}$; $V_{\text{bgs-P}} = 120\% \times \text{VDD}$) is tested, the internal power increases greatly in SG mode. While in LP mode, it also increases, but hardly as much as that in SG mode.

4.4 Output load

Output load is another interpolation index of look-up-tables in bulk-silicon MOSFET power library model. In power library model for FinFET, output load is also an important influencing factor for internal power. As shown in Figure 7, LP-mode circuits consume less internal power compared to SG-mode for the difference in threshold voltage (the back-gate bias voltage is $V_{\text{bgs-N}} = -20\% \times \text{VDD}$; $V_{\text{bgs-P}} =$

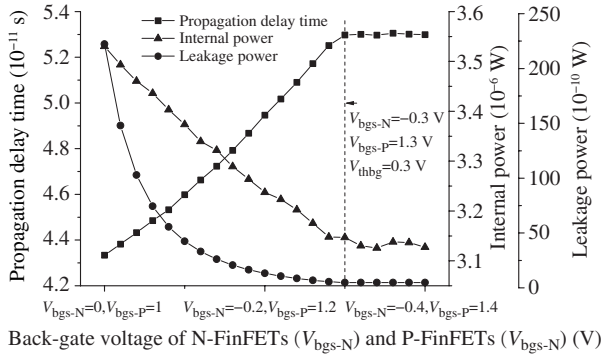

Figure 5 Back-gate bias voltage vs. power and delay. An LP-mode inverter is tested. Input slew is 0.1ns. When the internal is tested, the output load is 0.0048726 pF. When leakage is tested, output load is null. And the back-gate bias voltage affects both leakage power and internal power.

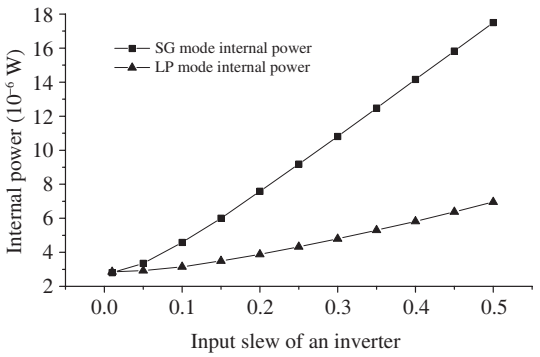

Figure 6 Input slew vs. internal power. Other conditions are as same as Figure 4.

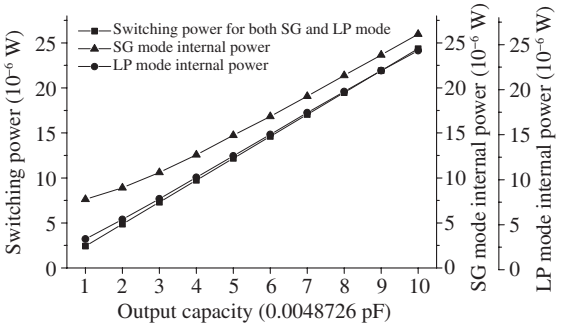

Figure 7 Output load vs. internal power. 0.0048726 pF is input capacitance of an inverter. The output load Fan-out varies from 1 to 10.

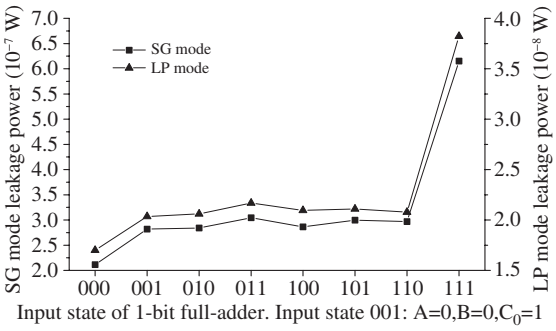

Figure 8 State vs. leakage power. The test is based on a 1-bit full-adder.

120% × VDD). The switching power in Figure 7 is measured, and the result is coherent to (4). This prove that (4), which allows to calculates the switching power with a known output load.

The mechanism by which internal power increases almost to the same extend as switching power is also inferred. When the output voltage rises and the node capacitance gets charged. Here, the power consumption from power supply is $C \times \mathrm{VDD}^2$, there into, of which half is stored in the node capacitance, and the other half is dissipated through the effective resistance of current path from power to ground.

4.5 State

The leakage power varies according to input states [17,18]. In order to get a relatively accurate leakage in small-scale circuits, we tested a 1-bit full-adder. In Figure 8, the leakage power of SG-mode circuits of a 1-bit full-adder is greater than ten times of that of LP-mode circuits. Different static states result in different leakage power: the leakage power of state '111' in SG and LP mode is nearly 3 and 2 times than that of state '00' respectively. Thus in the FinFET power library model, leakage power according to static states should be included.

4.6 Previous state

Simulation results show that the internal power is related to previous input states. As shown in Table 2, previous state contributes to different internal power. The reason may due to the impact of the internal parasitic capacitance of the circuits.

Table 2 Internal power of a LP-mode inverter. The clock cycle is 2 ns. Pre-state is state just one cycle before. Other conditions are as same as Figure 4

Pre-state	State	Internal power (W)
0	Rise	2.9452E−7
Fall	Rise	3.0193E−7
1	Fall	4.3578E−7
Rise	Fall	4.3834E−7

Table 3 Internal power of a LP-mode two-input NAND. The Input B is connected to the N-FinFET close to GND. The input slew is 0.1 ns. Delayed rise and fall is 0.05 ns delayed

Input mode	Input A	Input B	Internal power (W)
Single action	1	Rise	1.7975E−7
	Rise	1	1.1231E−7
	1	Fall	4.1840E−7
	Fall	1	3.5616E−7
Synchronous action	Rise	Rise	1.6388E−7
	Fall	Fall	4.7197E−7
Delayed multi-action	Rise	Delayed rise	2.4586E−7
	Delayed rise	Rise	1.8513E−7
	Fall	Delayed fall	4.4576E−7
	Delayed fall	Fall	5.0159E−7
Conflicts	Fall	Rise	3.3175E−7
	Rise	Fall	3.8173E−7
	Fall	Delayed rise	9.6567E−8
	Rise	Delayed fall	1.6698E−6
	Delayed fall	Rise	1.6218E−6
	Delayed rise	Fall	8.1778E−8

4.7 Timing action

Every node in the circuit has four signal types: 0, 1, rise, fall, so a gate with n input ports, has 4^n input states. The impact of timing action on the power is discussed here. Table 3 shows every possible timing action and its internal power. Even in single action, different port's actions to different power consumptions. Therefore timing action must be considered for accurate power estimation.

4.8 Temperature

FinFETs have confined channel, surrounded by silicon dioxide, which has lower thermal conductivity compared to bulk silicon. This results in increased self-heating and aggravated thermal issues [9,19].

$$P_{\text{leakage}} = \text{VDD} \times I_{\text{static}} = \text{VDD} \times (I_{\text{gate}} + I_{\text{sub}}). \tag{7}$$

Eq. (7) calculates for leakage power. Although both sub-threshold leakage current (I_{sub}) and gate leakage current (I_{gate}) are known to vary with temperature, I_{sub} is by far more sensitive to temperature variation. At room temperature, I_{gate} is comparable to I_{sub}, however, at high temperatures sub-threshold leakage power becomes the dominant component of total static power consumption and the contribution of gate leakage becomes negligible [20]. I_{sub} can be expressed by:

$$I_{\text{sub}} \approx \mu_{\text{eff}} C_{\text{ox}} \frac{W}{L}(m-1)\left(\frac{kT}{q}\right)^2 \mathrm{e}^{-qV_t/mkT}, \tag{8}$$

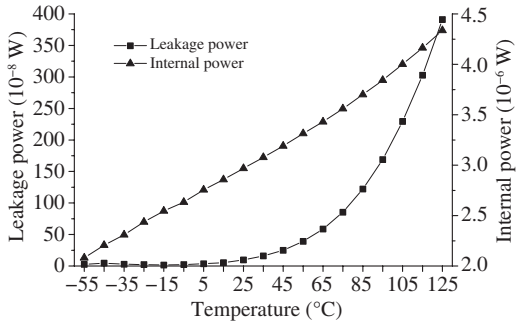

Figure 9 Temperature vs. power. A two-input SG-mode NAND is tested. The internal power is measured when the output load capacitance is charged. The leakage power is tested when $A = B = 1$.

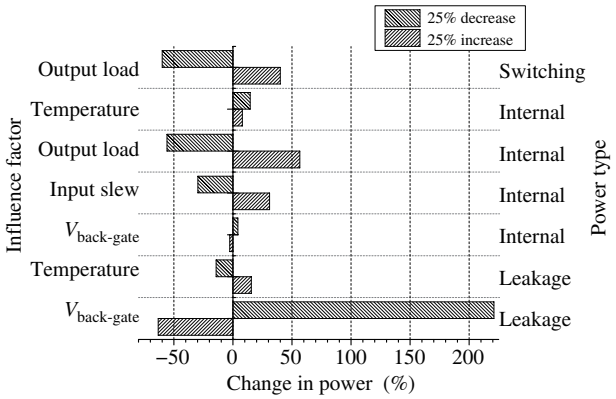

Figure 10 Sensitivity of different power type vs. influence factors.

Table 4 Selected sensitivity analysis elements

Elements	Normal	+25%	−25%
$V_{\text{back-gate}}$ ($V_{\text{bgs-N}}/V_{\text{bgs-P}}$)	−0.2 V/1.2 V	−0.3 V/1.3 V	−0.1 V/1.1 V
Input slew	0.3	0.4	0.2
Output load	5	8	2
Temperature	25°C	65°C	−15°C

where m is the body-effect coefficient. The temperature dependency of I_{sub} is dominated by $\mathrm{e}^{-qV_t/mkT}$ term since T^2 is compensated $\mu_{\text{eff}} \propto T^{-3/2}$. The high temperatures increases I_{sub} (which is a strong function of temperature T, $\mathrm{e}^{-qV_t/mkT}$, further increasing temperature T. If heat is not dissipated effectively, a positive feedback between leakage power and temperature can result in thermal runway [21,22].

Leakage and internal power with temperature of military standard is tested in Figure 9. The result demonstrates that temperature affects the leakage exponentially and internal power nearly linearly [23].

5 Analysis and discussion

The accuracy of power model can be improved by:

Key Characterization Factors of library. To discover and compare the factors that may influence power analysis accuracy.

Trace out the factors that may influence that power seriously, and use interpolation to estimate them, while making the less important factors other parameters. By using this method, the accuracy could be tremendously improved, while maintaining the speed of power analysis engine.

Improve the dimension of the look-up-table such as leakage power and internal power look-up-tables.

In Figure 10, One-way Sensitivity Analysis Method is used to weigh the influence that each factor has on detailed power. Table 4 lists out the elements selected for the test. In this process, several factors (mode, static state to leakage power; mode, pre-state and timing action to internal power) are removed for their difficulty of judging normal state and range. Although they are omitted in this sensitivity analysis, this does not mean they are not important to power model.

In Figure 10, as to leakage power, there are two factors listed: $V_{\text{back-gate}}$ (in this part, it stands for $V_{\text{bgs-N}}$ and $V_{\text{bgs-P}}$) and *temperature*. $V_{\text{back-gate}}$ influences leakage increasingly, while the *temperature*'s influence on leakage is much weaker. In this case, for key characterization factors for FinFET, $V_{\text{back-gate}}$ should be used as an important factor and be regarded as one of the index of the look-up-table for leakage power. The revised new look-up-table should be based on '*state*' and '$V_{\text{back-gate}}$' as shown in Figure 11 and Table 5. The newly added $V_{\text{back-gate}}$ index factor makes the leakage much more accurate, as can

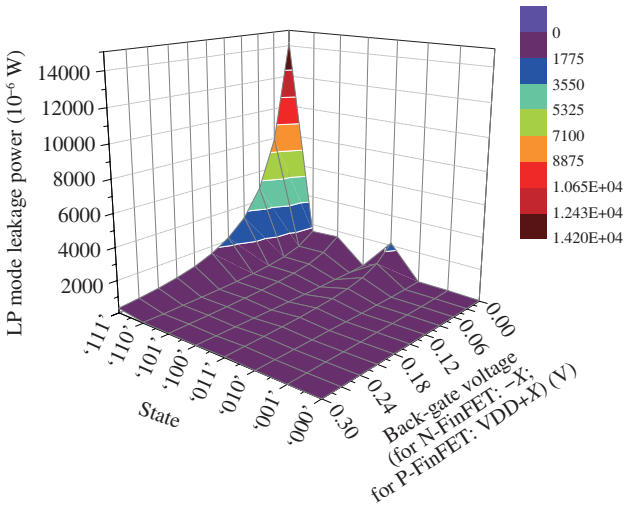

Figure 11 Revised Look-up-table for leakage power with index of '*state*' and '$V_{\text{back-gate}}$'.

be seen especially when in state '111' and $V_{\text{back-gate}} = 0$ ($V_{\text{bgs-N}} = 0; V_{\text{bgs-P}} = \text{VDD};$). In this way, the accuracy of leakage power estimation of FinFET is improved.

The *input slew* and *output load* are significant to internal power as shown in Figure 10, which corresponds to existing library in Table 1, where Look-up-tables are only indexed by these two factors. Different from 2-D MOS, the $V_{\text{back-gate}}$ and *temperature* are essential to FinFET internal power. As to *temperature*, the physical designer should pay more attention in order to prevent thermal run-away. Moreover, various low-power design methods should be applied. When it comes to $V_{\text{back-gate}}$, it is advisable to be used as one of the index labels for internal power, as shown in Figure 12. By improving the internal power look-up-table from 2-D to 3-D in Table 5, the accuracy of internal power estimation can be improved. As can be seen from Figure 12, the new added $V_{\text{back-gate}}$ factor can improve the accuracy of internal power especially with large *input slew* and *output load*.

Switching power can be calculated according to (4). In order to calculate the *output load*, netlist and wire load model are required. Thus FinFET switching power in Table 5 is similar to Table 1, both of which have only one index: *output load*.

Apparently there are several key modifications in Table 5 when compared to Table 1: The lookup table depth is extended from 7 to 10, because the factor-to-power variation for FinFET is larger than that in conventional bulk CMOS. Instead of using a parameter for leakage for each input state in Table 1, FinFET leakage look up table in Table 5 has two indexes: one is traditional input state, the other is backgate voltage of FinFET, because the backgate voltage feature impacts the FinFET leakage to a large extent as shown in Figures 10 and 11. The look up table for FinFET internal power in Table 5 is a three-dimension one, with backgate voltage feature included.

The more sensitive is some detailed power to one factor, the more should the factor be used as index of Look-up-table. As discussed above, in order to improve the accuracy of power model, the dimension of Look-up-table should be extended for FinFET as proposed in Table 5.

In case of discrete factors, like *mode*, *state*, *previous state* and *timing action*, different methods should be applied: To solve the difficulty caused by *mode*, libraries with different modes should be built as different cells. *Previous state* and *timing action* factors should be combined with the simulation waveform, especially in conditions that glitches may happen [24], which will significantly aggrandize the internal power dissipated.

Furthermore, according to the simulation results in this paper, we also suggest:

1) Choice of sampling points (this includes the number of sampling points, like 7 point in Table 1, and interval between two sampling points) is of great importance to accurate power estimation. In order to improve the accuracy, FinFET power library model in Table 5 has 10 sampling points since the wider the range, the larger numbers of sampling points, although smaller numbers of sampling points can bring

Table 5 Proposed FinFET standard cell power library model

```
//temperature
  temperature (25, Centigrade);
//part of the units
  capacitive_load_unit(1, pf);
  leakage_power_unit: 1uW;
//part of the library
  power_lut_template(pwr_tin_oload_vbackgate_10 × 10 × 10) {
    variable_1: input_transition_time;
    variable_2: total_output_net_capacitance;
    variable_3: back_gate_voltage;
    index_1("1, 2, 3, 4, 5, 6, 7, 8, 9, 10");
    index_2("1, 2, 3, 4, 5, 6, 7 8, 9, 10");
    index_3("1, 2, 3, 4, 5, 6, 7, 8, 9, 10");
  }
  lu_table_template(tmg_ntin_10) {
    variable_1: input_net_transition;
    index_1("1, 2, 3, 4, 5, 6, 7, 8, 9, 10");
  }
//one of the standarded cells
  cell(NAND2B_X0P5M_A12TS_FinFET) {
    area: x;
    cell_footprint: x;
    leakage_power() {
      related_pg_pin: "VDD";
      when: "!AN&!B";
      leakage_index(vbackgate_10) {
        index_1("x,x,x,x,x,x,x,x,x,x");
        values("x,x,x,x,x,x,x,x,x,x"); }
    }
...
    pin(AN) {
      capacitance: x;
      direction: input;
      fall_capacitance: x;
      input_voltage: default;
      max_transition: x;
      related_ground_pin: VSS;
      related_power_pin: VDD;
      rise_capacitance: x;
...
      internal_power() {
        related_pin: "B";
        when: "!AN";
        fall_power(pwr_tin_oload_vbackgate_10 × 10 × 10) {
          index_1("x,x,x,x,x,x,x,x,x,x");
          index_2("x,x,x,x,x,x,x,x,x,x");
          index_3("x,x,x,x,x,x,x,x,x,x");
          values(("x,x,x,x,x,x,x,x,x,x","x,x,x,x,x,x,x,x,x,x","x,x,x,x,x,x,x,x,x,x","x,x,x,x,x,x,x,x,x,x",
          "x,x,x,x,x,x,x,x,x,x","x,x,x,x,x,x,x,x,x,x","x,x,x,x,x,x,x,x,x,x","x,x,x,x,x,x,x,x,x,x",
          "x,x,x,x,x,x,x,x,x,x","x,x,x,x,x,x,x,x,x,x"),("x,x,x,x,x,x,x,x,x,x","x,x,,x,x,x,x,x,x,x,x",
          "x,x,x,x,x,x,x,x,x,x","x,x,x,x,x,x,x,x,x,x","x,x,x,x,x,x,x,x,x,x","x,x,x,x,x,x,x,x,x,x",
          "x,x,x,x,x,x,x,x,x,x","x,x,x,x,x,x,x,x,x,x","x,x,x,x,x,x,x,x,x,x","x,x,x,x,x,x,x,x,x,x"), ... ); }
...     }
```


faster calculating speed.

2) Different interpolation methods can be used to improve accuracy. For instance, exponent interpo-

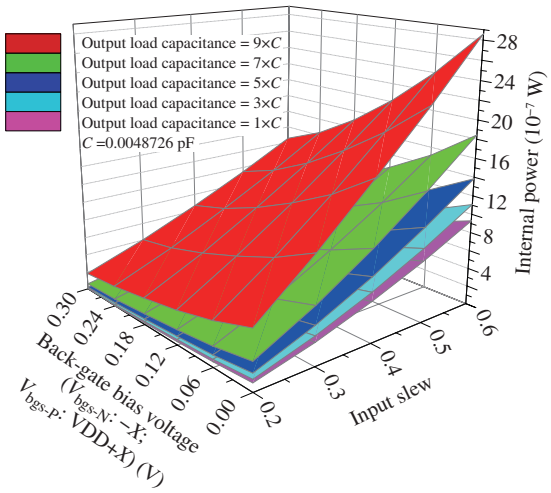

Figure 12 Revised Look-up-table for internal power with index of '*input slew*', '*output load*' and '$V_{\text{back-gate}}$'.

lation method can be used for temperature's influence to leakage power, especially after 55°C. Different temperatures lead to different power libraries: Table 5 is for 25°C.

6 Conclusion

This paper examines the possible factors that may influence FinFET power and compares the sensitivity between them. Based on the simulation results, a novel FinFET power library model is proposed. The work lays foundation for FinFET power model and power analysis engine.

The present study strongly recommends that the *mode* be taken as a separate factor because of its discontinuity. Different power libraries with different working modes should be built for FinFET circuits. *Previous state* and *timing action* should be combined with timing model. Accurate power analysis of high-performance FinFET circuits for dynamic power adjustment technology could be supported according to back-gate bias voltage.

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